Read Disturb Errors in MLC NAND Flash Memory: Characterization, Mitigation, and Recovery

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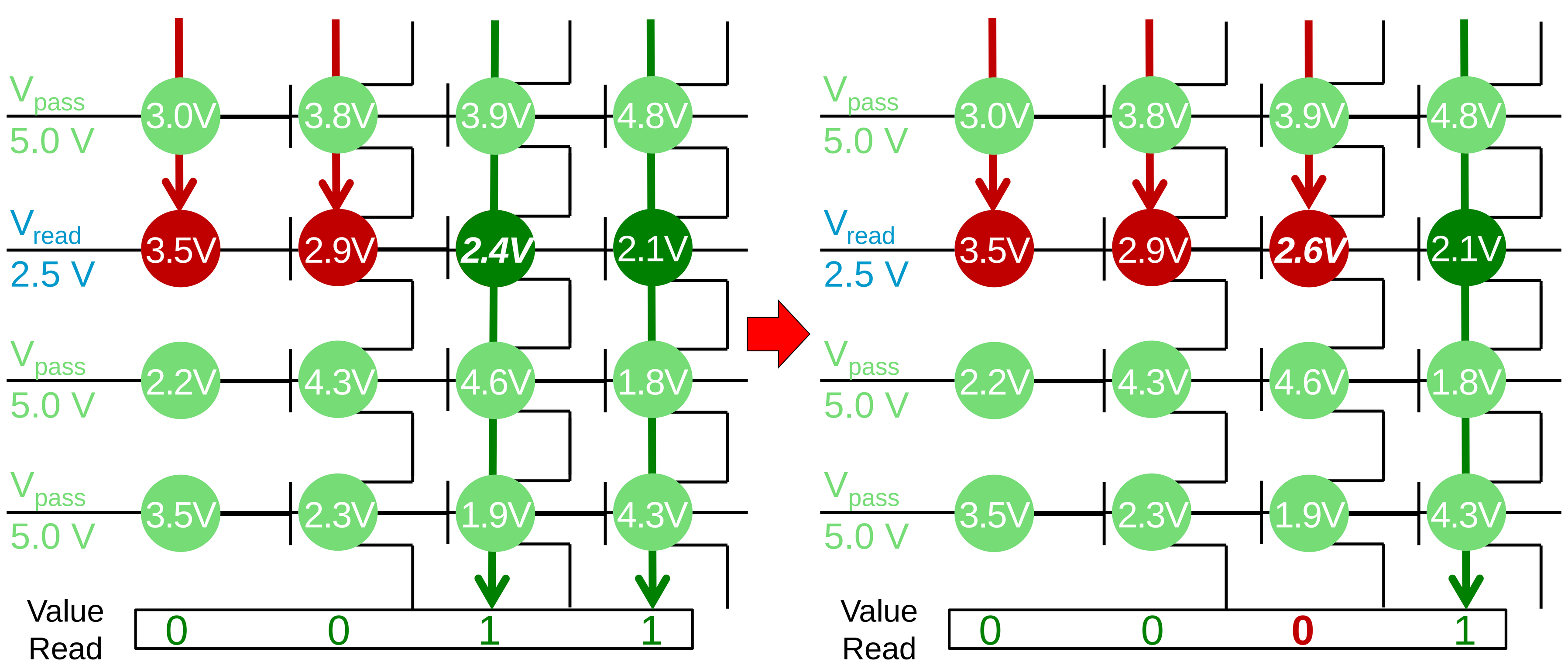
Overview

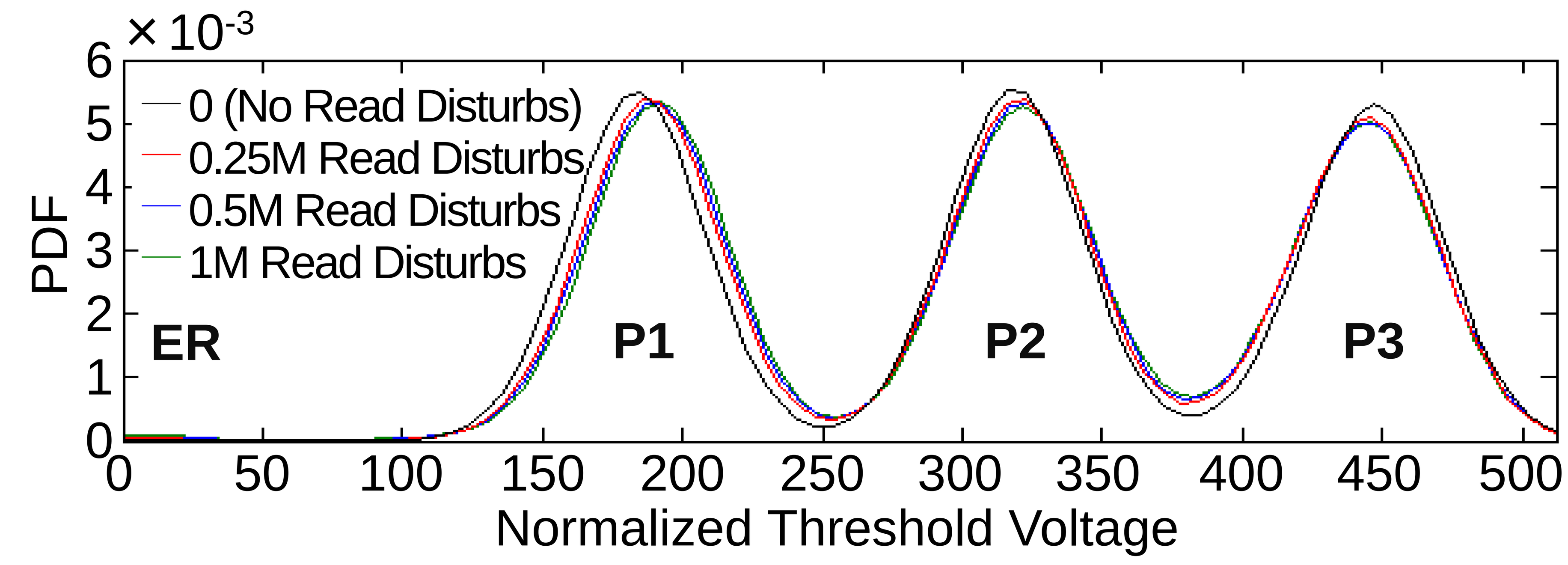
- Within flash block, when one page is read, V_{pass} (*pass-through voltage*) applied to other pages
- Pass-through voltage has a **weak programming effect** – in unread pages, stored voltages increase over time: ***read disturb***



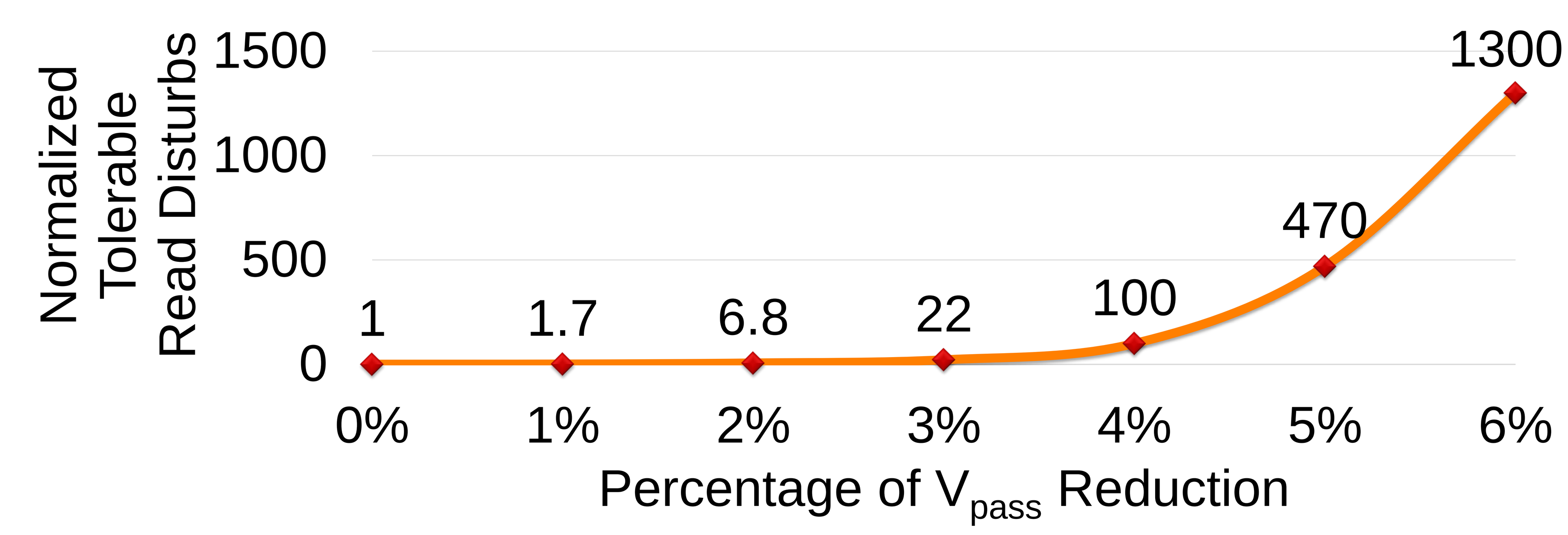
- **Characterize** impact of read disturb errors on *real 2Y-nm flash chips*
- Two solutions for read disturb
  - ***Mitigation*** by performing dynamic V_{pass} Tuning
  - ***Recovery*** by reversing read disturb behavior

Read Disturb Characterization: Real Chips

- Lower voltage states shift more as read disturb counts increase due to greater F-N tunneling

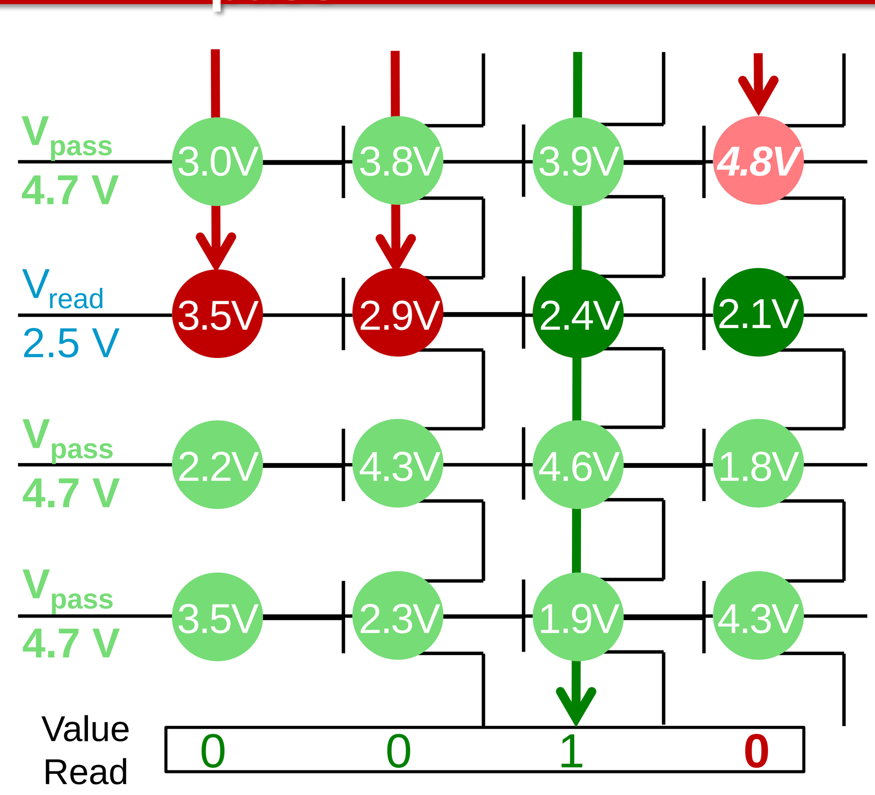


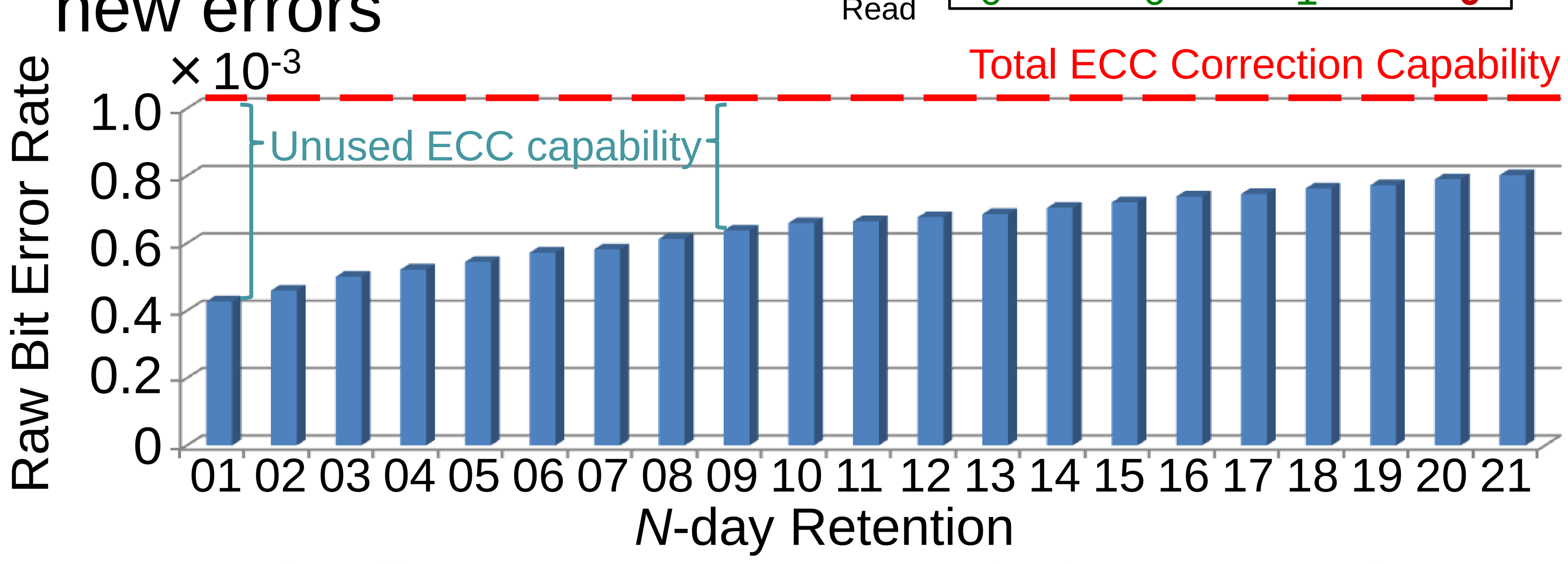
- Wear-out increases effect of each read disturb
- *Slightly* lowering V_{pass} *greatly* reduces read disturb errors



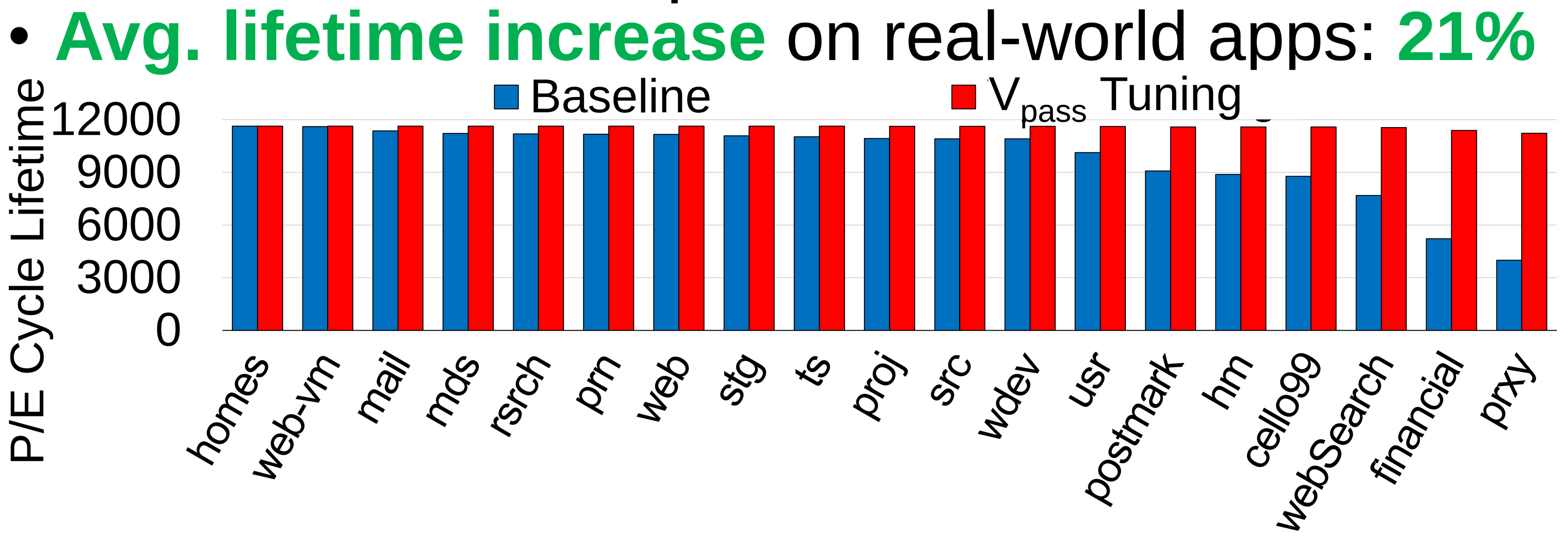
Read Disturb Mitigation: V_{pass} Tuning

- Lowering V_{pass} reduces read disturb errors, but **can introduce new read errors** – *improper pass-through*
- **Exploit unused ECC capability** to correct the new errors



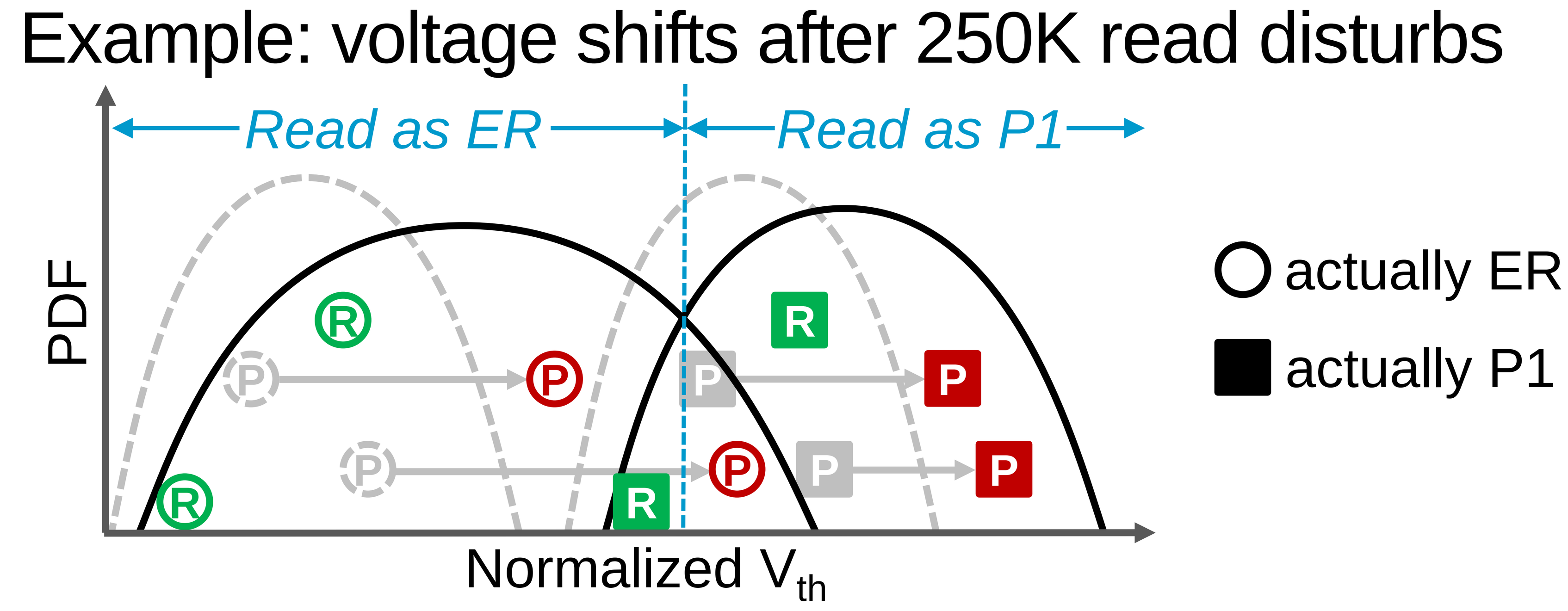


- **Dynamically tune V_{pass}** to maximize unused ECC
- **Avg. lifetime increase** on real-world apps: **21%**



Read Disturb Oriented Error Recovery

- Some flash cells *more susceptible* to read disturb
  - **Disturb-prone cells (P)**: large voltage shifts to high end of state distribution
  - **Disturb-resistant cells (R)**: small shifts, remaining in low end of distribution
- Example: voltage shifts after 250K read disturbs



- State boundary shifts: **cells now incorrectly read**
- Once flash lifetime ends (too many errors for ECC), recover data by *reversing read disturb*
  - Induce more read disturbs to ID prone/resistant
  - Predict *prone cells* → *lower state*
  - Predict *resistant cells* → *higher state*
  - ECC handles remaining corrections
- After 1M read disturbs, **recovery can reduce error count by 36%**

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