EE 42/43/100 Lecture/Readings/Lab Schedule (updated July 31, 2012)

Lecture	Date	Lecture Topics and Assignments	Reading	Lab
1	6/18	Introduction. Elementary concepts of voltage, current, power, DC vs. AC, series vs. parallel. KVL and KCL. Sources and resistive networks.	Ch 1, 2.1-3	Lab 1: Soldering
2	6/20	Review of resistive circuits. Node-voltage analysis. Mesh-current analysis.	Ch 2.1-5	
3	6/22	Review of nodal and mesh analysis. Source transforms; Thévenin & Norton equivalents. Maximum power transfer. Superposition. **HW 0 due.**	Ch 2.4-8	
4	6/25	Basic amplifier concepts. Voltage, current, power gain. Loading effects, cascaded amplifiers. Amplifier models and ideal amplifiers.	Ch 11.1-6	Lab 2: Resistive Circuits
5	6/27	Ideal op amps. Negative feedback. Inverting and noninverting amplifiers. Simple amplifier design. **HW 1 due.**	Ch 14.1-4	
6	6/29	Nonperiodic waveforms. Intro to capacitors and inductors. DC steady state.	Ch 3.1-5	
7	7/2	Review of first-order ODEs. RC and RL circuits. Integrators and differentiators.	Ch 4.1-4, 14.9	Lab 3: Op Amps
-	7/4	No lecture (holiday)	-	
-	7/5	**HW 2 due.**	-	
8	7/6	Second-order RLC circuits. Sinusoidal signals. **Quiz 1.**	Ch 4.5, 5.1	
9	7/9	Complex analysis, phasors, impedances, phase relationships. KCL and KVL.	Ch 5.1-4	Lab 4: Light Gate
10	7/11	Review of phasors and circuit analysis. Thévenin & Norton equivalents, max power transfer, superposition. Complex power. **HW 3 due.**	Ch 5.4-6	
11	7/13	Review of complex power. Fourier analysis, transfer functions. First-order filters. Introduction to Bode plots.	Ch 6.1-5	
-	7/16	**Midterm exam**	-	Lab 5: RC Timer
12	7/18	Bode plots. Higher-order filters, resonance. **HW 4 due.**	Ch 6.6-8	
13	7/20	Active filters and filter design. Diode physics. Shockley equation. Load-line analysis. Ideal diode model. Zener diodes. Piecewise-linear models.	Ch 10.1-5	
14	7/23	Wave-shaping circuits. Small-signal model.	Ch 10.6-8	Lab 6: Filters
15	7/25	MOSFET physics. Regions of operation. Load-line, bias, large-signal analysis. **HW 5 due.**	Ch 12.1-3	
16	7/27	Small-signal equivalents of MOSFET amplifiers. Common source configuration.	Ch 12.4-6	
17	7/30	Review of SS model, common source, common drain. Intro to digital logic and binary numbers. **Quiz 2.**	Ch 7.1-2	Lab 7: Boost Converter
18	8/1	Combinatorial logic. Boolean algebra, truth tables. NAND/NOR sufficiency. SOP, POS, logic mimimization. **HW 6 due.**	Ch 7.3-5	
19	8/3	Review of combinatorial logic. CMOS implementation of digital circuits. Intro to sequential logic circuits.	Ch 12.7	
20	8/6	Review of sequential logic. Latches, flip-flops, shift registers, counters.	Ch 7.6	Lab 8: ADC
21	8/8	Final review. **HW 7 due.**	-	
-	8/10	**Final exam**	-	

*Topic may or may not be covered depending on time.