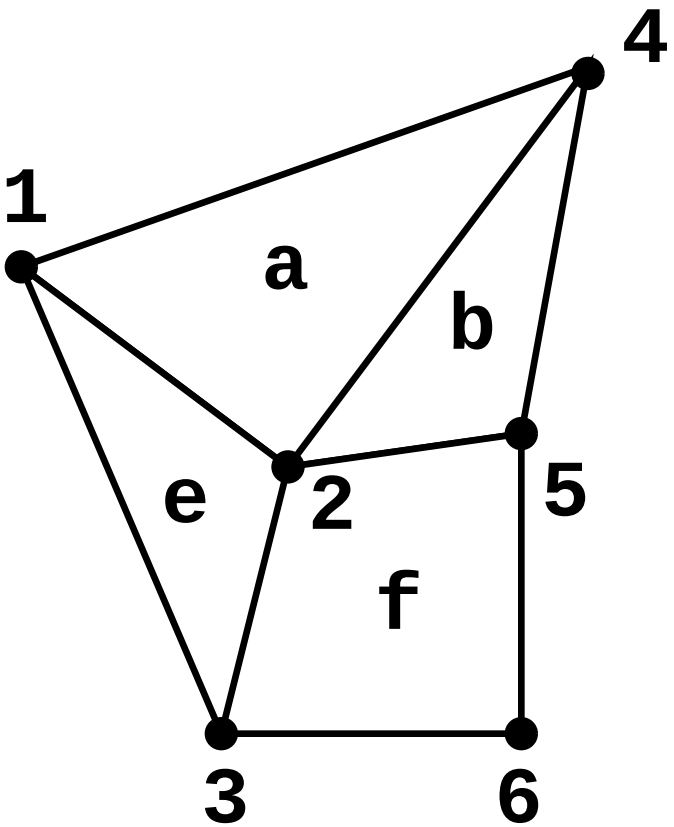
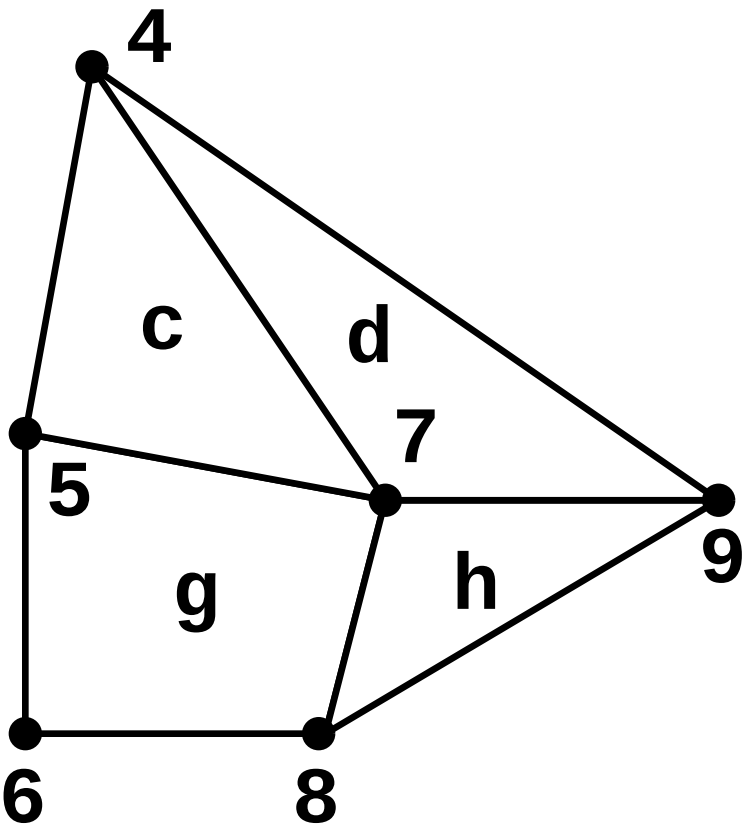
Processor 1



$$
\begin{array}{c|cccccc}
 & 1 & 2 & 3 & 4 & 5 & 6 \\
\hline
1 & X & X & X & X & & \\
2 & X & X & X & X & X & X \\
3 & X & X & X & & X & X \\
4 & X & X & & X & X & \\
5 & & X & X & X & X & X \\
6 & & X & X & & X & X
\end{array}
$$

K_1

Processor 2



$$
\begin{array}{c|cccccc}
 & 4 & 5 & 6 & 7 & 8 & 9 \\
\hline
4 & X & X & & X & & X \\
5 & X & X & X & X & X & \\
6 & & X & X & X & X & \\
7 & X & X & X & X & X & X \\
8 & X & X & X & X & X & X \\
9 & & & & X & X & X
\end{array}
$$

K_2