Computational Aspects of the Pipelined Phase-Rotation FFT
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Langhorne P. Withers, Jr., John E. Whelchel
E-Systems, Inc., Melpar Div.
7700 Arlington Boulevard
Falls Church, VA 22046

David R. O'Hallaron, Peter J. Lieu
School of Computer Science
Carnegie Mellon University
5000 Forbes Ave, Pittsburgh, PA 15213

Presenting Author:
David R. O'Hallaron

Corresponding Author:
David R. O'Hallaron
School of Computer Science
Carnegie Mellon University
5000 Forbes Avenue
Pittsburgh, PA 15213

phone: (412) 268-8199
fax: (412) 681-5739
email: ohallaron@cs.cmu.edu

Abstract

The phase-rotation FFT has a simple, constant-geometry, parallel-pipeline architecture. This paper considers computational aspects of implementing the FFT on a parallel computer system. Shuffle address and twiddle recipes, described directly in terms of the pipeline, are provided, and a recent full-bandwidth implementation on the iWarp parallel computer system is described. A new, parallel-pipeline equivalent of the index-reversing shuffle is added to complete the original phase-rotation FFT design.