NSF Science and engineering workshop

Nanocomputing design science challenges

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Thesis

- **Conventional scaling of CMOS will end in near term (10 to 15 years)**
- **That will be followed by a period of heterogeneous integrations of dissimilar technologies on silicon based platforms in the intermediate term (10-20 years)**
- **Finally, radical new scalable information processing technologies will emerge in the far term (> 20 years)**

Goal

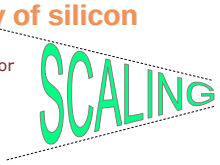
- **Define the design sciences required to integrate novel information processing technologies with existing computational infrastructure in an evolutionary manner**

Outline

- CMOS forever
  - Scaled silicon and the ITRS
  - The foundations of scaling
  - The economics of scaling
  - CMOS device circa 2015
- Alternative technologies
  - A universe of options
  - Selection criteria
- Age of integration –CMOS + other stuff
- Conclusions

The beauty of silicon

For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by



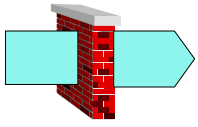
1. Scaling device dimensions downward
2. Scaling wafer diameter upward

	1990	1995	2000
DRAMs	4 MB	64 MB	1 GB
Feature size	0.8 µm	0.35 µm	0.15 µm
Wafer diameter	6"	8"	12"
Cost per Megabit	$6.50	$3.14	$0.10

Source: ICE

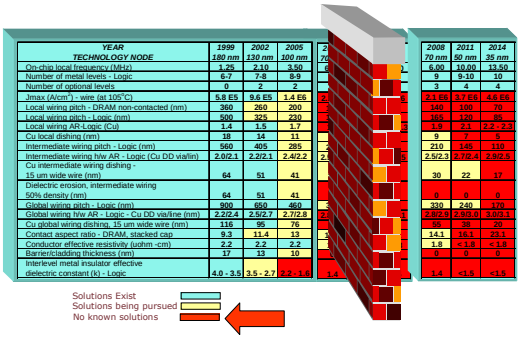
Scaling will get harder

- For the ***first time***, scaling appears to have reached fundamental limits in several areas.
- Current ITRS contains several major barriers ("brick walls") with ***no known solutions***.
- Barriers are approaching fast with the acceleration of the ITRS over the past 5 years.
- Overcoming these barriers will require:



- ***New*** materials
- ***New*** types of devices
- ***New*** physical models
- ***New*** types of processing
- ***New*** design tools & methodology

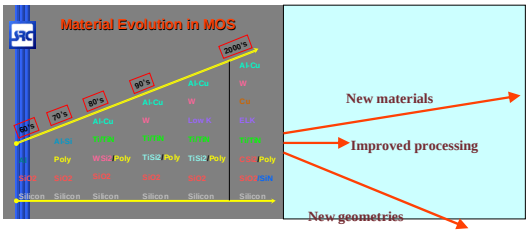
Brick Walls on the ITRS



YEAR	1999	2002	2005	2008	2011	2014
TECHNOLOGY NODE	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
On-chip local frequency (MHz)	1.25	2.10	3.50	6.00	10.00	13.50
Number of metal levels - Logic	6-7	7-8	8-9	9	9-10	10
Number of optional levels	0	2	2	3	4	4
Jmax (A/cm²) - wire (at 105°C)	5.8 E5	9.6 E5	1.4 E6	2.1 E6	3.7 E6	4.6 E6
Local wiring pitch - DRAM non-contacted (nm)	360	260	200	140	100	70
Local wiring pitch - Logic (nm)	500	325	230	165	120	85
Local wiring AR-Logic (Cu)	1.4	1.5	1.7	1.9	2.1	2.2 - 2.3
Cu local dishing (nm)	18	14	11	9	7	5
Intermediate wiring pitch - Logic (nm)	560	405	285	210	145	110
Intermediate wiring h/w AR - Logic (Cu DD via/lin)	2.0/2.1	2.2/2.1	2.4/2.2	2.5/2.3	2.7/2.4	2.9/2.5
Cu intermediate wiring dishing - 15 um wide wire (nm)	64	51	41	30	22	17
Dielectric erosion, intermediate wiring 50% density (nm)	64	51	41	0	0	0
Global wiring pitch - Logic (nm)	900	650	460	330	240	170
Global wiring h/w AR - Logic - Cu DD via/line (nm)	2.2/2.4	2.5/2.7	2.7/2.8	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing, 15 um wide wire (nm)	116	95	76	55	39	29
Contact aspect ratio - DRAM, stacked cap	9.3	11.4	13	14.1	16.1	23.1
Conductor effective resistivity (uohm -cm)	2.2	2.2	2.2	1.8	< 1.8	< 1.8
Barrier/cladding thickness (nm)	17	13	10	0	0	0
Interlevel metal insulator effective dielectric constant (k) - Logic	4.0 - 3.5	3.5 - 2.7	2.7 - 1.6	1.4	<1.5	<1.5

Solutions Exist
Solutions being pursued
No known solutions

The economic imperative



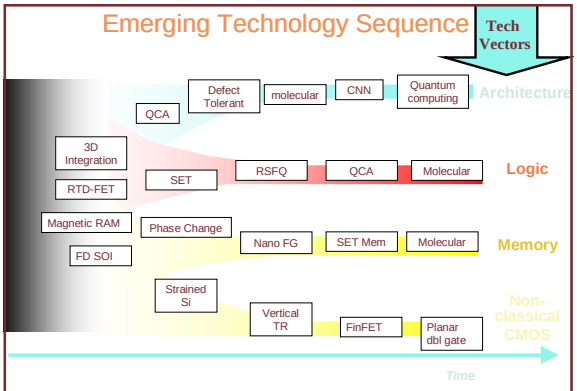
Scaling Will continue as long as
(δ cost) /(δ performance) > alternate technologies

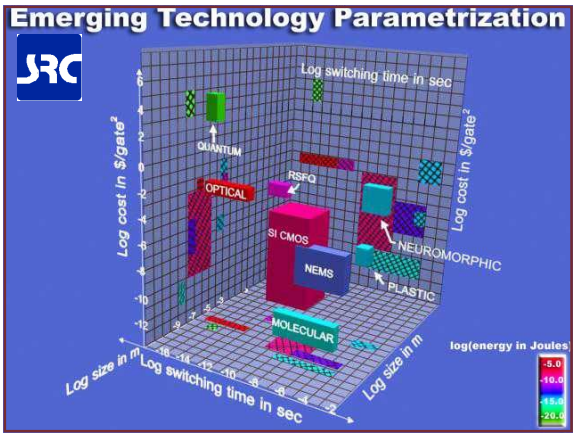
CMOS device circa 2016

- **Cost** 10^{-11} $/gate
- **Size** 8 nm / device
- **Speed** 0.2 ps /operation
- **Energy** 10^{-18} J/operation

Alternative technologies

Emerging Technology Sequence





Which technologies will dominate?

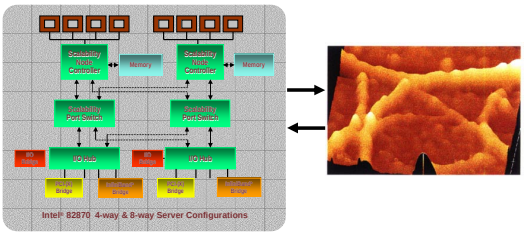
- Economic relevance criteria
  - The risk adjusted ROI for any new technology must exceed that of silicon
- Caution
  - Sufficiently advanced technologies will create their own applications. New technologies cannot necessarily be justified by current day applications.

Which technologies will dominate? What are the selection criteria?

- ***Energy efficiency***
- ***CMOS compatibility***
- ***Performance***
- ***Scalability***
- ***Architectural compatibility***
- ***Sensitivity to parametric variation***
- ***Room temperature operation***
- ***Stability and reliability***

Age of integration

The challenge



Changing architectural paradigms

Current

- Boolean logic
- Binary data representation
- 2D
- Homogeneous
- Globally interconnected
- Synchronous
- Von Neuman
- 3 terminal

Future

- Neural networks, CNN, QCA,…
- Associative, patterned, memory based, … data representations
- 3D
- Non homogeneous
- Nearest neighbor
- Asynchronous
- Integrated memory/logic
- 2 terminal

System software design needs to facilitate emerging technologies

Challenge

- CMOS is based on Boolean logic and binary data representation
- Alternative technologies will require “native” logic systems and data representations to optimize their performance

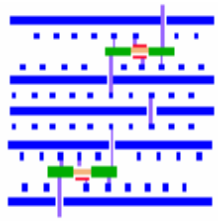
Solution?

- Design science must provide functional abstractions and interfaces to couple multiple, dissimilar technologies into a single functional system

Emerging Research Architectures

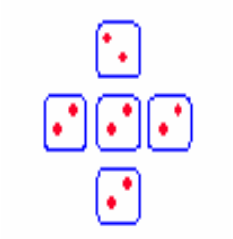
Architecture	3-D Integration	Quantum Cellular Automata	Defect Tolerant Architecture	Molecular Architecture	Cellular Nonlinear Networks	Quantum Computing
Device Implementation	CMOS with dissimilar material systems	Arrays of quantum dots	Intelligently assembles nanodevices	Molecular switches and memories	Single electron array architectures	Spin resonance transistors, NMR devices, Single flux quantum devices
Advantages	Less interconnect delay, Enables mixed technology solutions	High functional density. No interconnects in signal path	Supports hardware with defect densities >50%	Supports memory based computing	Enables utilization of single electron devices at room temperature	Exponential performance scaling, Enables unbreakable cryptography
Challenges	Heat removal, No design tools, Difficult test and measurement	Limited fan out, Dimensional control (low temperature operation), Sensitive to background charge	Requires pre-computing test	Limited functionality	Subject to background noise, Tight tolerances	Extreme application limitation, Extreme technology
Maturity	Demonstration	Demonstration	Demonstration	Concept	Demonstration	Concept

Heterogeneous 3D integration



- 3D integration
  - Shorter interconnects
  - High aerial density
  - Thermal management
  - Test and measurement
- Heterogeneous integration
  - Integration of new devices
  - Difficult interfaces
  - Manufacturing issues
  - Lack of design tools

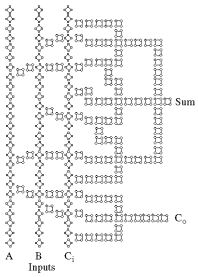
Quantum cellular automata



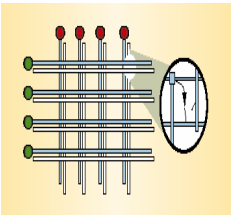
- Local interconnection
  - High density
  - Self assembly
  - No interconnects in signal path
  - Limited fan out
  - Sensitive to stray charge
- Asynchronous
  - No clock signal
  - Logic complexity

Quantum Cellular Automata

Floating adder executed with Quantum Cellular Automata (U. Notre Dame)

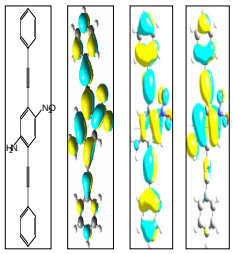


Fault tolerant architecture



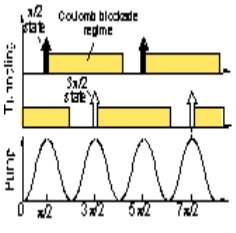
- Integration of imperfect devices
- Two terminal devices
  - Consistent with self assembly, bio technology
- Lack of gain
- Requires pre testing
- High interconnect density

Molecular architecture



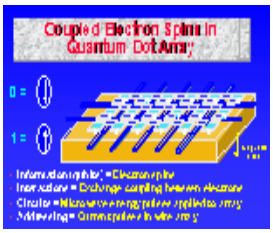
- Supports new charge transport mechanisms
- Supports self assembly
- Requires memory based logic
- Primarily 2 terminal logic

Tunneling Phase Logic



- Local interconnections
- Supports RTD integration
- Non charge encoded logic and signaling
  - Electrical phase
  - Low transition energy
  - Multi-valued logic
  - Requires pump signal
- Sensitive to stray charge

Quantum computing



- Non charge encoded logic and signaling
  - Quantum phase information
- New applications
- Exponential speedups
- Secure information transmission
- Extreme sensitivity to everything

Conclusions

- Scaled CMOS will dominate microelectronics for next 15 years and provide the common platform indefintely
- Alternative technologies will require native logic systems and data representations to be developed
- Integration and market acceptance will require functional abstraction and transparent interfaces