Mock CMOS: An Inexpensive, Fast, and Versatile Microfabrication Technique Using One Metal and One Silicon Dioxide Film

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Abstract

A versatile fabrication process that allows users to quickly construct micromachined structures using a one metal, one silicon dioxide film stack on a silicon wafer is presented in this technical report. This simplified process, called Mock CMOS, (a) starts from pre-processed wafers and requires only one photolithography step, (b) provides a conductor material for actuating electrostatic and thermal devices, (c) avoids electrical shorting between metal microstructures or to the silicon substrate by using silicon dioxide as an insulator, and (d) allows quick prototyping of MEMS structures similar to those designed at Carnegie Mellon University (CMU).

The CMOS-MEMS process at CMU is a post-CMOS fabrication process in which the etching masks are provided by the interconnect metal layers in the standard CMOS process. Prototyping of sensor and actuator devices in the CMOS-MEMS process requires considerable cost, waiting time for chip fabrication, and possible further iterations until satisfactory device performance is attained. By using the three fundamental materials of metal, oxide, and silicon, a designer can create microelectromechanical devices in the Mock CMOS process, similar to the standard CMOS-MEMS microstructures, yet with a significantly reduced turnaround time. By removing the CMOS component and limiting the process to one metal and one oxide layer, a designer can focus on the mechanical aspects of a microstructure with the capability to layout multiple device variations of arbitrary size onto a four inch wafer. The deposition of two layers (aluminum and silicon dioxide) on a batch of silicon wafers, along with lithography material costs, brings the price for Mock CMOS to $\$0.05/mm^2$.

Devices successfully created include surface-normal and lateral electrostatic and thermal actuators, the majority of which were designed by forty students in an Introduction to MEMS course in Fall 2001 at Carnegie Mellon University.

Introduction

This microfabrication technique arose due the need for a quick design-to-device turnaround for the CMOS-based micromachining technique developed at Carnegie Mellon University (CMU) [1]. Carnegie Mellon has developed an integrated CMOS-MEMS process in which microstructures with high-aspect-ratio composite-beam suspensions are fabricated using conventional CMOS processing along with a sequence of maskless dry-etching steps. The etching masks are provided by the interconnect metal layers in the standard CMOS process. Advantages of this process include the ability to integrate low-noise sensor interface circuitry, feedback control, signal amplification and processing alongside microstructures. By regulating the combination of three metal and one polysilicon layers, a designer is able to create fourteen types of varying thickness microstructures along with the ability to use vias to interconnect these layers. Unfortunately a standard design-to-device cycle using *MOSIS* (MOS Implementation Service), a production service for VLSI circuit development, typically takes 2-3 months after design submission and costs $5000 for twenty-five small dies with an area less than 5 mm^2, any additional area costs $1,180/$mm^2$ [2]. Figure 1 shows the individual post-CMOS processing steps needed to create a cantilever beam composed of three metal and one polysilicon layers in the CMOS-MEMS process. Prototyping of sensor and actuator designs in the CMOS-MEMS process requires considerable cost for a small die area along with significant waiting time for chip fabrication, which hinders fast prototyping.

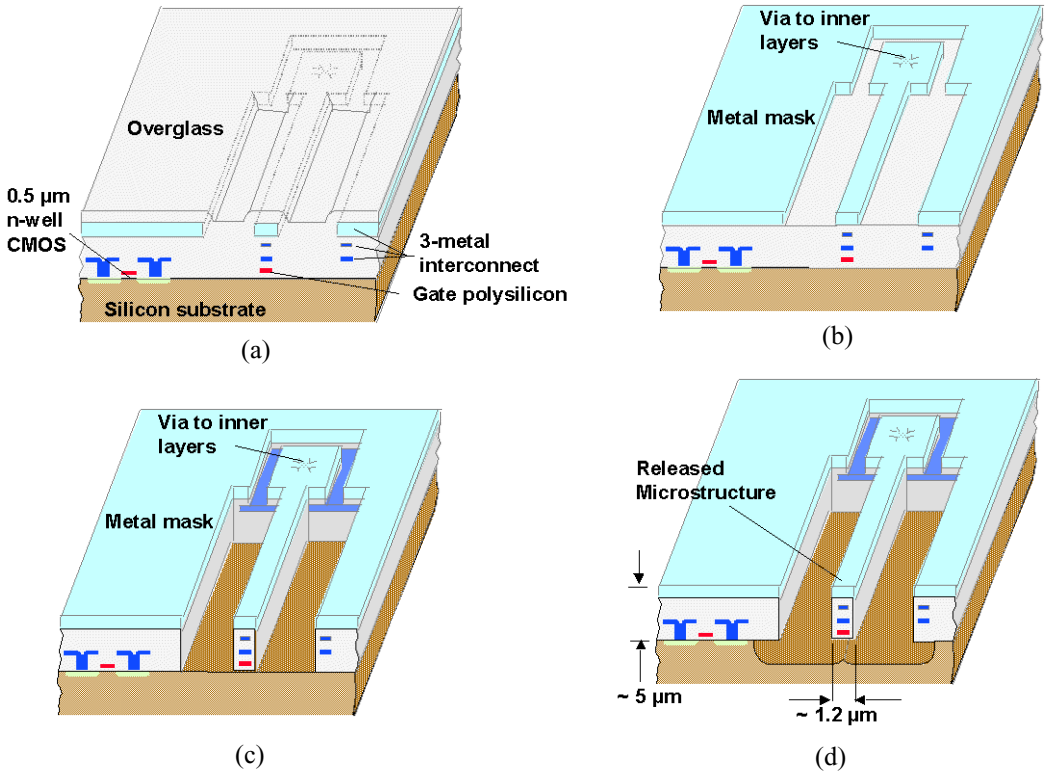


Figure 1: Schematic of the process flow for micromachined structures in standard CMOS process flow. (a) Chip shown as received from CMOS foundry. (b) Reactive ion etch of the top overglass oxide down to top metal mask. (c) Completion of reactive ion etch and definition of microstructure sidewalls. (d) Released structure after silicon isotropic etch. Note: Metal layers are made of aluminum. Titanium tungsten barrier metal not shown.

Photo courtesy Xu Zhu

The Mock CMOS process is shown in Figure 2. Using just a metal and oxide film stack on a silicon wafer, one is able to create similar microstructures as those produced in the CMOS-MEMS process, following equivalent post-CMOS fabrication steps. Yet by removing the CMOS component, a designer can place more focus on the mechanical aspects of the sensor or actuator with a lower cost and shorter turnaround. In addition, the designer is not limited by die area since the Mock CMOS process is a full wafer process, this allows the freedom to layout multiple

design variations on a single wafer. The ability to use large wafer real estate for a lower cost allows the integration of macro devices, such as fiber optics or fluidic tubing, which tend to require significant die area.

Starting from pre-processed silicon wafers, with each film thickness matching the specifications of metal/oxide microstructures under the standard CMOS-MEMS process, the design-to-device turnaround becomes only a week or less depending on photomask production time. Although it is only possible to create one of the fourteen different types of CMOS-MEMS microstructures, the Mock CMOS process could be used as a stepping stone before more complicated designs are attempted with the CMOS-MEMS process.

Figure 3 provides a structural comparison of the standard CMOS-MEMS process and the Mock CMOS process by observing the cross section. Figure 3a comes from the MOSIS Agilent 0.5 micron process after performing a anisotropic RIE of the silicon dioxide layer. Figure 3b shows the Mock CMOS process after performing aluminum, titanium tungsten, and silicon dioxide etches prior to microstructure release.

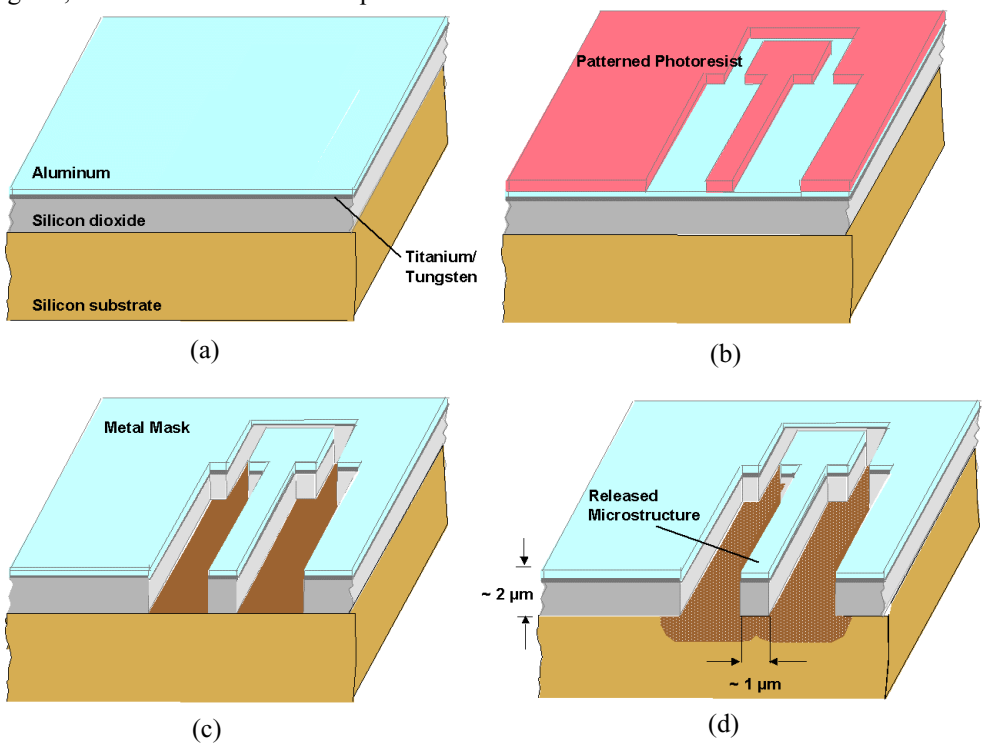


Figure 2: Schematic of the Mock CMOS process. (a) Starting point showing film stack as received from vendor. (b) Photoresist patterned above the aluminum film. (c) Reactive ion etch of the silicon oxide down to the silicon substrate (the photoresist is removed during the process). (d) Released structure after silicon isotropic etch.

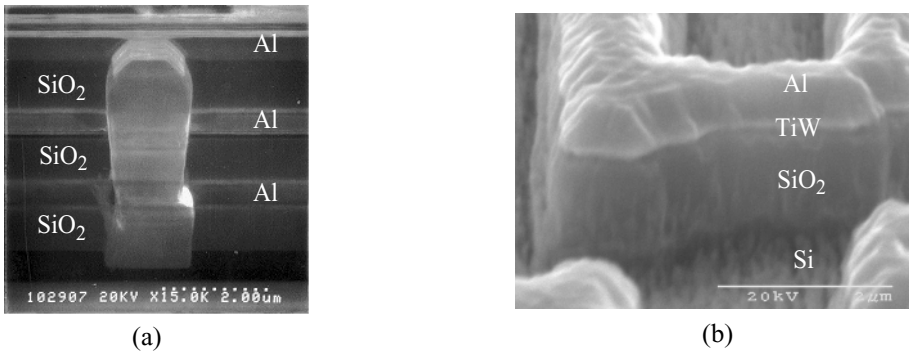


Figure 3: Cross section of CMOS-MEMS and Mock CMOS microstructure. (a) Three metal film stack from a *MOSIS Agilent* 0.5 micron CMOS process. (b) Cross section of a Mock CMOS microstructure before silicon etching. The bright white layer in both pictures is the titanium tungsten layer.

Wafer Specifications

Due to currently limited resources, wafers were purchased from an outside vendor with all three films (aluminum, titanium tungsten, and silicon dioxide) already deposited. In order to have a thermally grown oxide film on silicon, a furnace is needed with integrated capabilities to flow water vapor for a "wet" oxidation over a batch of 4-inch wafers. For the titanium tungsten deposition, a sputtering machine is needed with cosputtering capability in order to form a balanced alloy film. To prevent any particle contamination or possible native oxide growth from the titanium tungsten layer, the aluminum needs to be deposited immediately after the titanium tungsten without breaking vacuum in the sputtering process.

The pre-processed wafers were provided by *MEMS Exchange* (Reston, Virginia), an intermediary for various university and corporate fabrication centers. A batch of 4-inch diameter, <100> oriented, n-type, 500 micron thick, single-sided polished, prime quality silicon wafers were used for subsequent processing. Wafers need to be sufficiently conductive to use the substrate as an electrode for electrostatic actuation, therefore a resistivity in the 1..20 Ω-cm range was used. Type of dopant is not important. Subsequent effort should be made to use double-sided polished wafers for cases where backside resist patterning is needed, such as in deep reactive ion etching (DRIE).

To accurately mimic mechanical functionality of a conventional one metal and one oxide CMOS-MEMS die, it is critical that material properties and dimensions remain as accurate to the standard CMOS process. Each of the three films deposited above the silicon substrate matches the specifications of a one metal (Metal-1), one oxide microstructures under the standard *MOSIS Agilent* 0.5 micron process.

MEMS Exchange provides a thermal wet oxide on the polished wafer side, grown to a thickness of approximately 1.25 microns. The silicon dioxide film thickness on three different 24-wafer batch runs provided by *MEMS Exchange* has produced a varied set of numbers (1.17 micron, 1.28 micron, and 1.66 micron) according to spectrophotometric film measurement plots. A thermal wet oxide is used instead of low pressure chemical vapor deposition (LPCVD) oxide since this type of layer mimics the field oxide deposited during the local oxidation of silicon (LOCOS) process in a CMOS foundry to isolate transistors.

A 0.13 micron titanium tungsten layer was then deposited above the oxide layer. Titanium tungsten is used as a barrier metal in order to prevent junction leakage current in the CMOS process, but it's used in this process to emulate the film structure of a CMOS-MEMS device. This barrier metal is deposited by *Lance Goddard Association* (*LGA Films*), a *MEMS Exchange* fabrication site, that can perform the cosputter of titanium and tungsten.

Finally, a 0.44 micron thick aluminum film is also deposited by *LGA Films* above the titanium tungsten. As was mentioned, the aluminum is deposited immediately after the titanium tungsten without breaking vacuum in the sputtering process. Sputtering parameters used by *LGA Films* were using a power setting of 3 kW and pressure of 10 mTorr of Argon. The price for the three film depositions on a batch of twenty-four 4-inch silicon wafers costs $2000, based on February 2002 prices from *MEMS Exchange*.

Based on current prices for *MOSIS Agilent* 0.5 micron CMOS services and comparing it to material costs for pre-processed wafers and lithography, the price per CMOS die comes to $\$40/mm^2$ while for Mock CMOS the price per wafer comes to $\$0.05/mm^2$. The high price for CMOS is due to the numerous lithographic and processing steps needed to create transistors and their various interconnect.

Fabrication

Starting with the pre-deposited wafers, the fabrication process first begins with a lithography step that results in a patterned photoresist layer over the top aluminum film of the wafers. *Shipley* S1813 is the positive-tone thin photoresist often used at a thickness of 1.3 to 1.5 microns. This resist has been successfully used in contact alignment down to 1 micron features. The photoresist is spun at 4000 RPM for 30 seconds with an initial 6 second spread at 500 RPM. The softbake is conducted at 110° Celsius on a hotplate for 90 seconds. After wafer cooling, the resist is exposed for a total dose of 75 mJ/s^2. Development is performed for 1 minute using a 1:1 mixture of deionized water and *Shipley* Microposit Developer (a special developer that does not etch aluminum). Figure 4 shows a scanning electron micrograph of a photoresist patterned wafer.

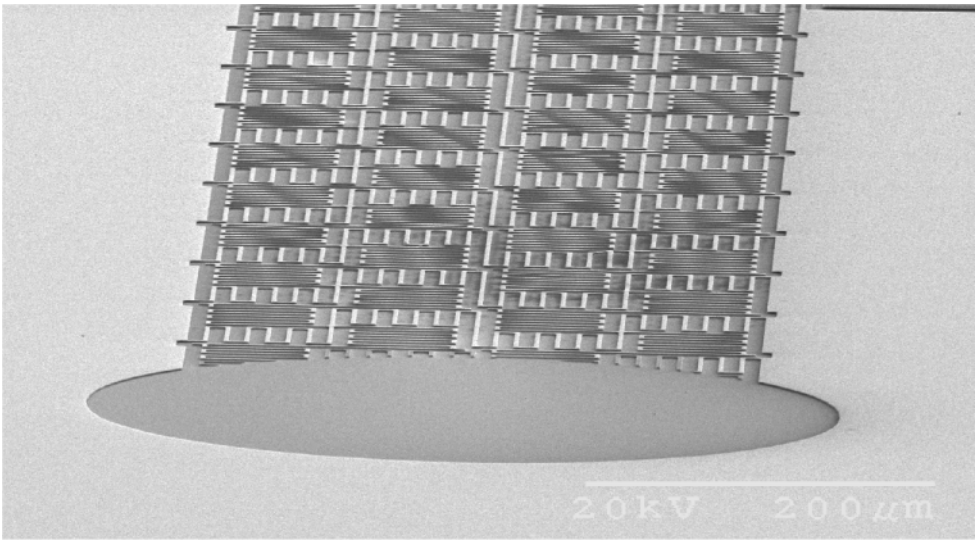
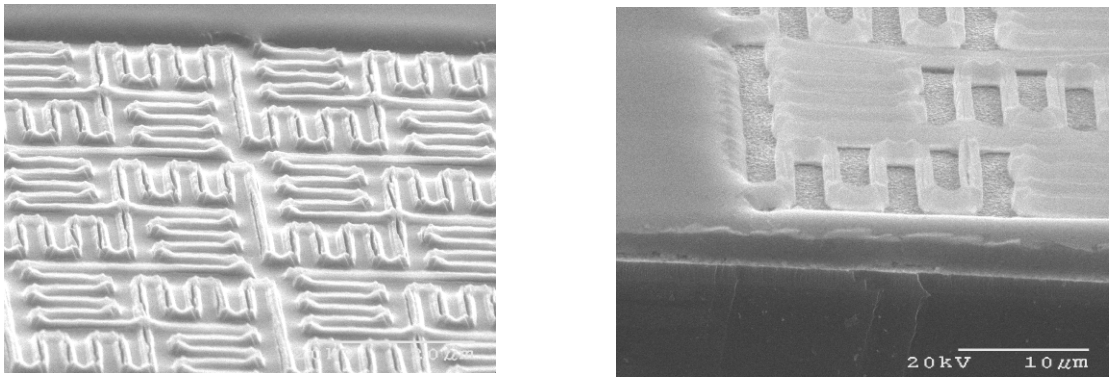


Figure 4: Micrograph showing the patterned photoresist layer over the top aluminum film.

A subsequent dry or wet etch removes the aluminum and titanium tungsten films. In this specific case a commercial wet aluminum etchant and hydrogen peroxide solution were used to remove the aluminum and titanium tungsten films, respectively. The aluminum etchant used was provided by *Transene Corporation* under the name-brand of *Type A Pre-mixed Aluminum Etchant*. The etchant is composed of phosphoric, acetic, and nitric acid mixture



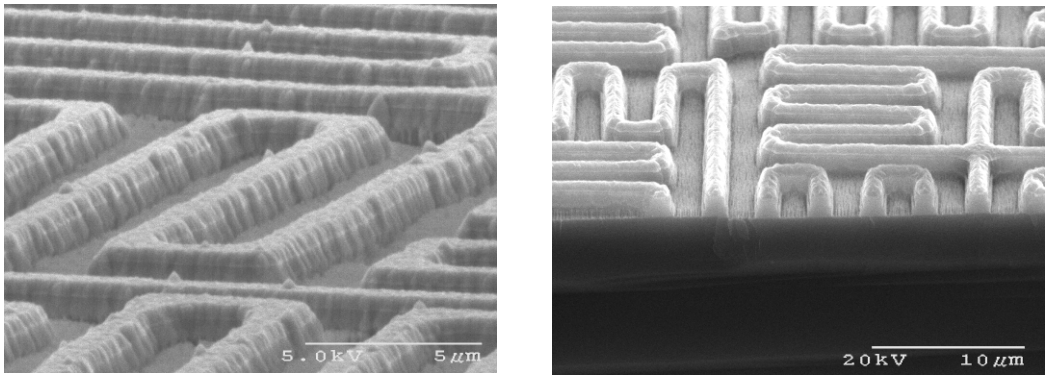
(a) (b)

Figure 5: Micrograph showing the Mock CMOS wafer (a) after aluminum etching with a pre-mixed commercial etchant and (b) after titanium tungsten etching with hydrogen peroxide.

along with a small part of deionized water. Any commercial hydrogen peroxide solution will perform the titanium tungsten etch. Both etches were performed at 45-50° Celsius baths to accelerate the etching (hot plate settings were at 70° Celsius). The advertised etch rate for the pre-mixed aluminum etchant at the stated temperature is 100 Angstroms

per second, while the titanium tungsten etchant has an etch rate of 20 Angstroms per second (as determined from visual inspection). The wafer was kept in the aluminum etchant for 40 seconds then rinsed in deionized water before being placed in the titanium tungsten etchant for 80 seconds. Figure 5a shows a micrograph after the wet aluminum etch, while Figure 5b shows a micrograph after the titanium tungsten etch using hydrogen peroxide.

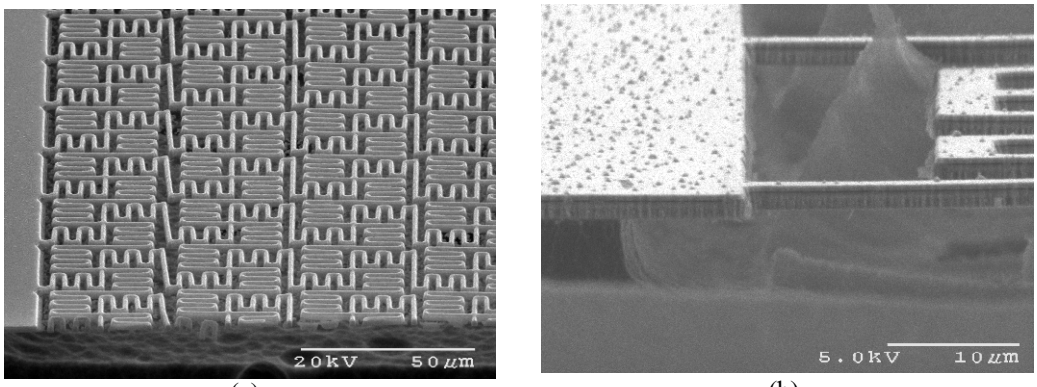
After the metal layers are patterned, the aluminum film is used as an etch-resistant mask during the subsequent etching that creates the microstructures (the photoresist layer, which was used as a mask for etching the metal layers, erodes during subsequent plasma processing). Silicon dioxide areas not covered by metal are anisotropically etched to create vertical sidewalls using a trichloromethane (CHF_3) and oxygen reactive ion etch (RIE) performed in a *Plasma Therm* 790 RIE system. The parameters used are 22.5 sccm flow of CHF_3 mixed with a 5 sccm flow of O_2, 100W power, 125 mTorr chamber pressure, for a 60 minute time interval. Figure 6 is a micrograph of a Mock CMOS wafer after the silicon dioxide etch. An advantage of using trifluoromethane (CHF_3) to etch the silicon dioxide layer is the benefit of a thin polymer passivation layer on the vertical sidewalls that deposits during the oxide etching. This prevents electrical shorting during in-plane actuation of microstructures.



(a) (b)

Figure 6: Scanning electron micrograph after performing anisotropic silicon dioxide etch using CHF_3/O_2 reactive ion etch. (a) After 30 minutes in the reactive ion etch system. (b) After completing the full 60 minute etch.

A final silicon etch, using xenon difluoride or any other silicon etchant, releases the microstructure. To reduce the amount of exposure time to plasma processing, xenon difluoride is the preferred etchant for the Mock CMOS process [3]. The xenon difluoride etch is performed on a *XACTIX* Xetch Xenon Difluoride Etch System. The parameters used for the etch are 3 Torr XeF_2 pressure, 0 Torr N_2 pressure, 15 cycles with each cylce time being 60 seconds (15 minute total etch time). Figure 7 is a micrograph showing the released microstructure after the silicon etch.



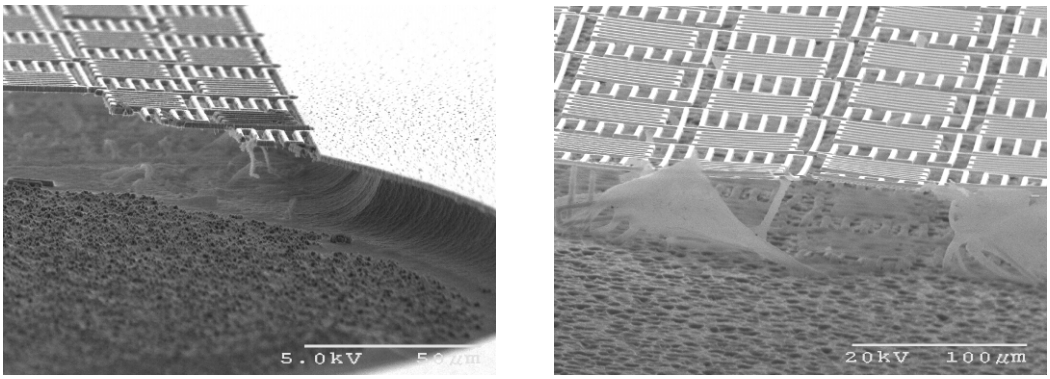
(a) (b)

Figure 7: Scanning electron micrograph after performing isotropic silicon etch using xenon difluoride for 15 minutes. (a) Lower magnification picture of a suspended membrane (b) Close-up micrograph near an anchor support.

Process Refinement

Minor adjustments were needed throughout the fabrication sequence until a fully functional device was created. One of the major problems involves performing full wafer processing instead of individual die processing, as is done with CMOS-MEMS dies. All of the material etching processes discussed (these include those for aluminum, titanium tungsten, silicon dioxide, and silicon) are dependent on the amount of material exposed to the etching species. This is often referred to the "loading effect" and is especially apparent in plasma etching processes. To alleviate this problem, full wafer was diced into smaller samples before reactive ion etching of the oxide film and subsequent silicon etching using xenon difluoride. This dicing process can lead to particulate accumulation on samples, which may cause occluding during etching processes.

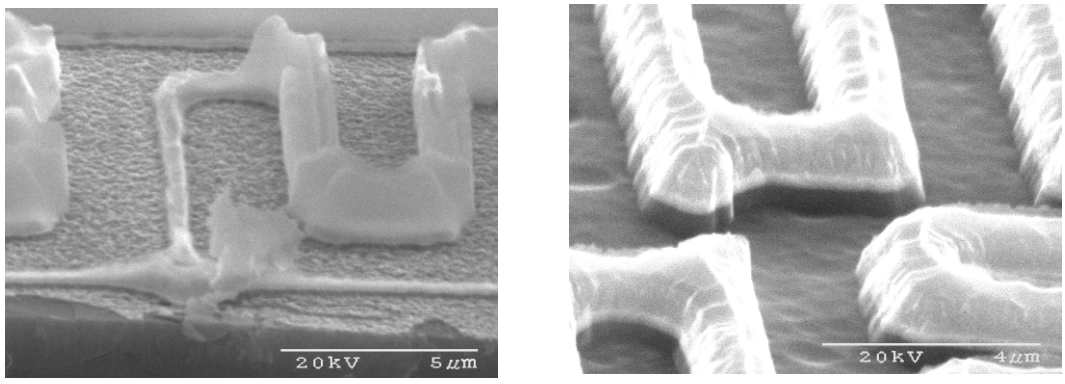
A significant problem during the reactive ion etching of silicon dioxide was the resputtering of aluminum onto the entire wafer. Aluminum has a low sputter energy therefore it can be easily redeposited when exposed to high energy ions, as in a reactive ion etch plasma cloud. Figure 11a shows small stringers that are dangling below the released microstructure while Figure 11b shows the large patches of a polymer-like film forming in the gaps between



(a) (b)

Figure 8: Micrographs depicting the aluminum redeposition problem. (a) Stringers can be seen under the suspended microstructure. (b) Large patches of a polymer-like film were seen in-between and under microstructures.

the microstructure. This polymer film has been analyzed by a fellow researcher using energy dispersive X-ray diffraction (EDX) and determined to contain aluminum, carbon, and fluorine[7]. To prevent this problem, the photoresist layer, that remains after metal patterning, was used to shield the aluminum from this plasma energy. Unfortunately the photoresist erodes during the ion bombardment but can be made to withstand this erosion by reducing the oxygen flow rate during the oxide RIE from the typical 16 sccm used in the CMOS-MEMS process to 5 sccm. In addition, by hard baking the photoresist layer, the resist forms a tough skin layer that makes it more difficult for oxygen to remove. Attempts were made to spin-on a thicker photoresist layer that could withstand longer plasma processing and protect the aluminum film. *Shipley* S1813 can be spun at 1000 RPM to create a ~2.5-3 micron thick pho-



(a) (b)

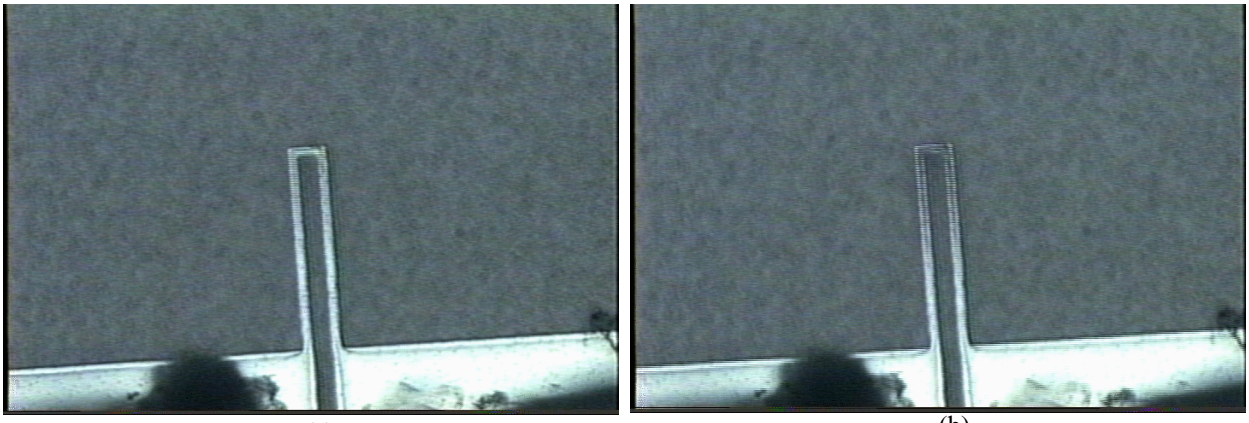
Figure 9: Comparison between wet etching and ion milling of metal layers (aluminum and titanium tungsten). (a) The photoresist layer is significantly degraded after being exposed to the wet chemical etchants. (b) The ion beam mill provides a cleaner profiler without a reduction in width.

toresist layer. Softbake was done for 90 seconds at 115° Celsius while exposure dose was 225 mJ/s^2. The thicker resist may cause difficulties in resolving fine features.

Wet etching of thin films, as during the metal layer patterning, has certain undesirable properties. The main problem lies in the isotropic nature of the wet etchant which will cause undercutting of the mask layer by the same distance as the etch depth. Therefore a 2 micron wide feature, after isotropically etching a 0.5 micron thick film, will become only 1 micron in width. Numerous features in our design mask have minimum feature size widths of 1.6 microns, therefore the timed wet etch must be precise in its definition or the feature will be lost. A dry reactive ion etch can perform an anisotropic etch with no mask undercutting. The resources for a dry reactive ion etch of the metal films was not available but the availability of an ion beam mill allowed an anisotropic profile. An ion beam mill works by physically bombarding the surface with high energy ions to etch films instead of using a chemical reaction, as reactive ion etching does. Figure 9 provides a comparison between a wet etched microstructure and an ion milled microstructure.

Results

Devices successfully created include surface-normal and in-plane electrostatic and thermal actuators, the majority of which were designed by forty students in an Introduction to MEMS course in Fall 2001 at Carnegie Mellon University. Thermal actuators were created by running a small current through a finite width metal loop which acted as a small resistor, Eagle et al. used this actuation for scanning tip microscopy in the CMOS-MEMS process [4]. The loop is basically two cantilever beams joined at their end. Figure 10a and 10b demonstrates an out-of-plane thermal actuator before and after passing 20 mA of current, respectively. The out-of-plane motion is demonstrated



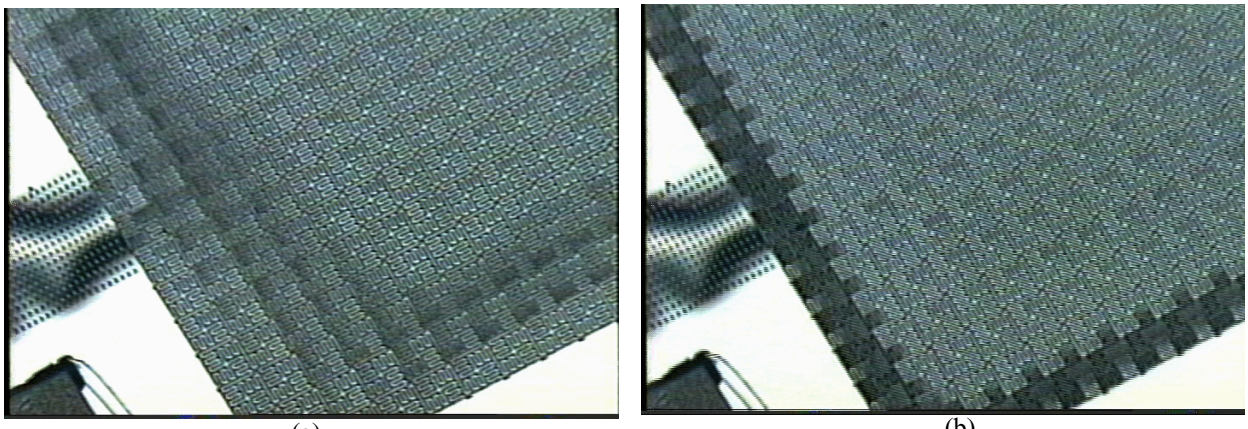
(a) (b)

Figure 10: Micrograph of an out-of-plane thermal actuator (two cantilever beams joined at the end). (a) The actuator without any current flow. (b) After a 20 mA current is applied. The out-of-plane motion is demonstrated with a loss of surface reflectivity from the aluminum surface.

Device courtesy S. Zadeh

with a loss of surface reflectivity from the aluminum surface. As this resistor heated up, the loop curled out-of-plane from the silicon wafer. After the current was turned off, the loop immediately cooled and dropped to its original position due to the low thermal mass of the structure. Its possible to create lateral movement thermal structures by having a different width around the loop; one of the cantilevers would have a larger width than the other.

Electrostatic actuators were demonstrated by creating a large flexible membrane based on a design by Neuman et al. [5]. The serpentine structure of the membrane allows the membrane to flex and touch the silicon substrate, the silicon dioxide layer underneath the metal provides insulation preventing any electrical shorting. Figure 11a and 11b shows the membrane before and after actuation with a 30 Volt DC bias. The short xenon difluoride etch allowed



(a) (b)

Figure 11: Micrograph of an out-of-plane electrostatic actuator based on a large suspended membrane. (a) The actuator without any voltage bias. (b) After a 30 Volt DC bias is applied. The out-of-plane motion is demonstrated with a loss of surface reflectivity from the aluminum surface on the outer membrane fringes.

the creation of a small gap below the suspended membrane (approximately 15 microns), thus allowing for a minimal actuation voltage.

The temperature dependent residual stress gradients that cause CMOS-MEMS microstructures to curl was successfully recreated using the Mock CMOS process as evidenced in Figure 12. Stresses in each of the three films deposited are temperature dependent, this is caused by the differences in thermal coefficient of expansion for each layer [6]. This problem was analyzed by Lakdawala et al. with the development of modelling tools to better predict when multilayer microstructures will curl.

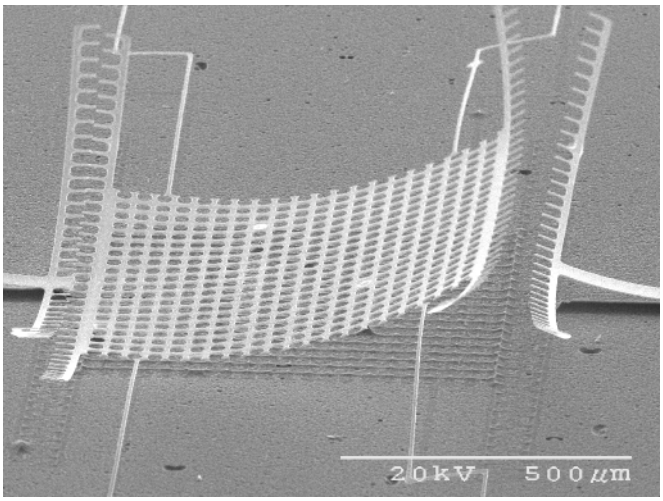


Figure 12: Micrograph showing the large residual stress gradient apparent in the multilayer resonator.

Future Work

To fully characterize microstructures created in the Mock CMOS process, we intend to use a similar process characterization that was done with the CMOS-MEMS process [8]. These test structures will allow the determination of effective Young's modulus and residual stress of a metal and oxide microstructure. The effective Young's modulus is determined by optically measuring the lateral resonance frequency of simple cantilever beams as shown in Figure 13. Residual stress will be measured using bent-beam strain sensors as shown in Figure 14 [9]. In addition, vertical stress gradient will be measured by measuring the out-of-plane radius of curvature for various length beams. Future work will also be done to develop a set of design rules to help designers during layout of various dimension micro-structures.

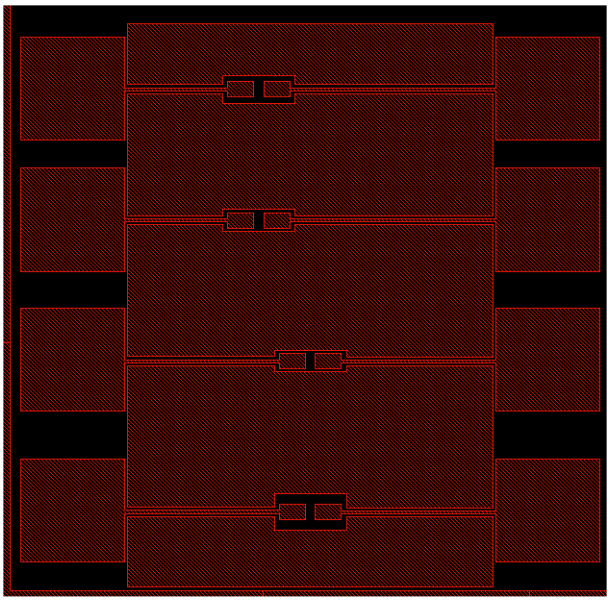


Figure 13: Layout of simple cantilever beams for determination of effective Young's modulus.

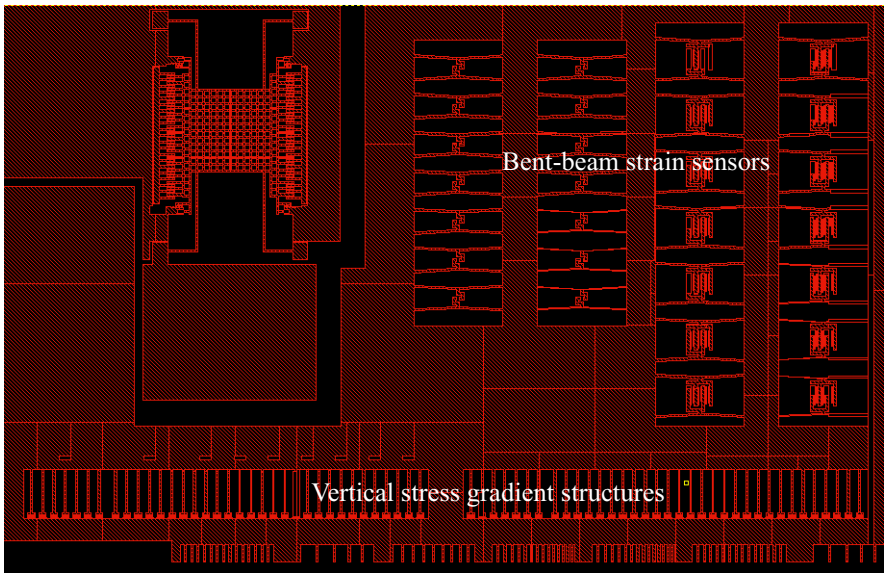


Figure 14: Layout of bent-beam strain sensors for determination of residual stress and various length beams for vertical stress gradient measurement.

Conclusion

The Mock CMOS process was presented as a simplified version of the CMOS-MEMS technology developed at Carnegie Mellon University. Users can quickly construct micromachined structures using a one metal, one silicon dioxide film stack on a silicon wafer with minimal cost, fast turnaround, and the availability of larger wafer real estate compared to the CMOS-MEMS process. By removing the CMOS component and limiting the process to one metal and one oxide layer, a designer can focus on the mechanical aspects of a microstructure with the capability to layout multiple device variations of arbitrary size onto a four inch wafer.

The report discussed some of the process refinements that were necessary to achieve successful device operation, these difficulties were mainly due to deleterious effects of processing four inch wafers. Some of the devices successfully created include electrostatic and thermal actuators, the majority of which were designed by forty students in an Introduction to MEMS course in Fall 2001 at Carnegie Mellon University. Future work will involve characterizing Mock CMOS microstructures as well as developing a set of design rules.

Acknowledgements

I would like to acknowledge my fellow MEMS colleagues for their help in developing the Mock CMOS process, especially Matte Zeleznik and Brett Diamond. Both Matte and Brett were teaching assistants during the Fall 2001 semester of the Intro. to MEMS course when the Mock CMOS process was used by 40 students for their final projects. I also appreciate the effort made by students in the course to develop interesting devices, some of which are highlighted in this paper. I would like to thank Xu Zhu for providing technical assistance during process refinement. I would like to thank my advisor, Dr. Ken Gabriel, for having enough confidence to use the process in the MEMS course and to continue funding the process.

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