Abhilasha Jain

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Interests

Computer Systems and Architecture, Designing efficient memory subsystems, hardware/software co-design

Education

Ph.D., Carnegie Mellon University
Computer Science 2018-present
Advisor: Prof. Phillip B. Gibbons

M.S., Carnegie Mellon University
Electrical and Computer Engineering 2016-2018

B.Tech., Manipal Institute of Technology
Electronics and Communication Engineering 2012-2016

Research Experience

Systems for Robotics and AI March 2018 - Present
- Exploring the computational challenges in AI and Robotics, specifically reinforcement learning.
- Motivating the need for specialized systems and architectures in such domains.

Cross-layer memory abstraction for enhanced performance and portability May 2017 - Dec 2017
- Motivated the need to express program semantics to OS and hardware to improve performance and portability.
- Designed and implemented new hardware caching and prefetching policies to leverage the additional software context.
- Achieved up-to 2.6x reduction in execution time for Polybench workloads compared to state-of-the-art.
- Demonstrated reduction in performance variance from 55% to 6% across different last-level cache sizes.

Publications

Nandita Vijaykumar, **Abhilasha Jain**, Diptesh Majumdar, Kevin Hsieh, Gennady Pekhimenko, Eiman Ebrahimi, Nastaran Hajinazar, Philip B. Gibbons and Onur Mutlu. *A Case for Richer Cross-layer Abstractions: Bridging the Semantic Gap with Expressive Memory*, International Symposium on Computer Architecture (ISCA) 2018

Abhilasha Jain, Dhananjay Sahoo, B. S. R. Sarvani, K. Sukumar, Ritvik Gupta, and Adheesh Boratkar, *Calibration and characterization of a COTS thermal camera for space*, Aerospace Conference 2016

Abhilasha Jain, and Chandrasekhar Nagarajan, *Efficient Control Algorithm for a Smart Solar Street Light*, International Conference on Next Generation Mobile Applications, Services and Technologies 2015

Projects

Code transformation to eliminate insignificant writes to NVMs Jan - May 2017
- Motivated write traffic reduction for machine learning applications on NVMs owing to NVM read-write asymmetry.
- Implemented compile time transformation in LLVM to eliminate insignificant writes.
- Reduced writes by 10% with a maximum overhead of 3% extra reads without any application code change.

Accelerating single source shortest path (SSSP) using processing-in-memory Jan - May 2017
- Designed an on-chip accelerator for in-memory graph processing using 3D stacked memory technologies.
- Developed a custom processing core and a specialized interconnect for efficient communication between the cores.
- Achieved a maximum of 8x run-time improvement for SSSP compared to a single-threaded CPU implementation.

Binary-tree searches using hybrid FPGA-CPU systems Aug - Dec 2016
- Accelerated binary tree searches using the Xilinx Zedboard All programmable SOC.
- Designed custom search kernels that run parallel searches on the FPGA.
- Converted a large binary tree into multiple smaller trees on an ARM CPU and then transferred to FPGA for search.

Co-Curricular Projects

Student satellite for thermal imaging Aug 2013 - Feb 2016
- Headed the payload subsystem responsible for the thermal imaging payload of the satellite.
- Lead the end-to-end interfacing, integration, calibration and qualification of a COTS Thermal Infrared Camera.

Work Experience

Renesas Electronics, Singapore: Embedded Design Intern Jan - May 2016

Bhabha Atomic Research Center, India: Project Trainee, Electronics Division June - July 2014

Skills

Languages: C, C++, Python, Verilog, Assembly(ARM, x86)
Tools/Simulators: PIN, ZSim, LLVM, MATLAB, Vivado HLS, Xilinx ISE

Relevant Coursework

Human-Computer Interaction, Planning in Robotics, Advanced Storage Systems, Graduate Computer Architecture, Optimizing Compilers for Modern Architectures, Foundations of Computer Systems