Scheduler Hardware

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The Scheduler is based on an Intel 960 CPU running at 34.56Mhz. It has access to an 8Kx16 dual port sram which it uses to communicate with the PCC.

Interrupts

There are two sources of interrupts to the Scheduler:
- The first is the Non Maskable Interrupt (NMI). It is generated by the Watch Dog Timer, when the Scheduler has not scheduled any cells for a period of one second.
- The second is the interrupt from the PCC. It is maskable by the Scheduler by setting or resetting a configuration bit. This interrupt will be configured as XINT0 on the CPU.

Resets

There are three sources of resets to the Scheduler:
- The Watch Dog Timer (WDT) - When the Scheduler has not scheduled any cells for a period of one second after the NMI, the WDT generates a reset to the Scheduler.
- The PCC - the PCC has control over the reset to the Scheduler. It uses this control and the setting up the IBR and boot code in the dual port sram to boot the Scheduler.
- The Power Up Reset (POR) - when the power first comes up, the POR hardware generates a clean reset for the Scheduler.

Watch Dog Timer

The Watch Dog Timer is a counter which watches the Scheduler to see that it is still running by resetting the counter every time a cell is scheduled. If no cells are scheduled in the period of one second, an NMI is generated to the CPU. If no cells are scheduled for an additional second, a reset is generated to the CPU. The WDT is turned on and off by the PCC.

Memory

The Scheduler has an 8Kx16 dual port memory, which is used for booting and for communication with the PCC. The memory is accessed as a 256 by 8 bit wide memory at location ffffff00h, and as a 8K by 16 bit wide memory at location 10000000h. This memory may be accessed as 8, 16 or 32 bit wide memory by the processor.

The dual port memory also contains eight semaphore registers. Each register is 1 bit wide and is accessed in a 32 bit wide region. The location of the registers is as follows:

register 0 - 40000000h
register 1 - 40000004h
register 2 - 40000008h
register 3 - 4000000Ch
register 4 - 40000010h
register 5 - 40000014h
register 6 - 40000018h
register 7 - 4000001Ch

Refer to the IDT Specialized Memories & Modules Data Book for a complete description on how to read and write the semaphores. The semaphores may be accessed 8, 16 or 32 bits wide at a time, although only the least significant bit holds data.

The Scheduler will be held off via wait states from accessing the dual port memory if the PCC is accessing the same location but started first. The same holds true in the other direction, that the PCC will be held while the Scheduler accesses the memory.

Registers

The Scheduler has two control bits which it may read and write at location 20000000h

- data bit 0 - this bit controls the interrupt from the Scheduler to the PCC. The Scheduler writes a 0 and then a 1 to this bit to generate the interrupt.
- data bit 1 - this bit is the mask bit for the interrupt from the PCC. If the Scheduler writes a 1 to this bit, the interrupts from the PCC will be masked off. Writing a 0 will turn the masking off and interrupts will be received.

Synchronization

The Scheduler has the ability to resynchronize itself to the frame pulse. At any time the Scheduler may read from location 60000000h, and it will be held by wait states until the Data Manager signals that it is no longer busy. This will always happen at the same place during the cell cycle so the Scheduler can know exactly what the time is in the cell period.

Status Handler Interface

The Scheduler can read and write to the two registers in the Status Handler:

SCH_SEL = 0 register - 30000000h
SCH_SEL = 1 register - 30000004h

Refer to the SCH-STA interface document for a full description of the contents of the registers. These registers must be accessed 32 bits wide at a time to ensure that the 0 wait state performance is maintained.