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ADVANCE INFORMATION

iWarp Microprocessor

- High Performance Design
  - –40 MHz clock
  - –100 MOPS parallel performance
    - 20MFLOPS floating-point and
    - 20MIPS integer operation
    - 20MOPS memory access
    - 40Mword communication I/O
  - –Full 32-bit and 64-bit floating-point operation
  - – 64-bit memory access
  - –Full IEEE 754 floating-point implementation
  - –CHMOS IV process technology
  - –Compensated 50-ohm pin drivers
- Full Hardware Support for Parallel Computation Systems
  - –Integrated hardware to support interprocessor communication
  - –Scalable system performance
  - –Balanced communication to computation ratio
- High Computational Density
  - –One component plus memory comprises compute cell
  - –3 x 5 inch circuit-board footprint
- Familiar Microprocessor Usage Models
  - –standard register-based programming model
  - –Short RISC-like single-function instructions
  - –Long multi-function instruction
  - –DMA to memory
- Extensive Development Support
  - –Full range of development systems including Single Board Array
  - –Both cell and array level support
  - –Optimized C and FORTRAN
  - –Symbolic debugger, linker, loader
  - –Parallel programming tool and library for image processing
- Extensive System Support
  - –Direct component-to-component communication connections
  - –271-pin PGA package
  - –Extensive on-chip debug/break features
  - –Serial system reporting unit