15-740 Computer Architecture, Fall 2007
Schedule for In-Class Discussions

Day 1: Tuesday, October 9, 2007

Transactional Memory: Supporting Large Transactions: Conventional designs for hardware-supported transactional memory can only handle transactions of a limited size: how can we extend this support to larger transactions?


Transactional Memory: Hybrid Hardware/Software Approaches: How can we combine software- and hardware-based transactional memory to get the best of both worlds?


Thread-Level Speculation: Recent work on optimistically exploiting thread-level parallelism.

Load Imbalance in Chip Multiprocessors: What is the impact of asymmetry in a CMP, and how can we efficiently support dynamic scheduling?


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<thead>
<tr>
<th>Topic</th>
<th>Time Slot</th>
<th>Discussion Leaders</th>
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<tbody>
<tr>
<td>TM: Large Transactions</td>
<td>12:00-12:20</td>
<td>Vijay Vasudevan, Hetu Kamichetty</td>
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<tr>
<td>TM: Hybrid HW/SW Approaches</td>
<td>12:20-12:40</td>
<td>Paul Zagieboylo, Severin Hacker</td>
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<td>Thread-Level Speculation</td>
<td>12:40-1:00</td>
<td>Xi Liu, Lei Li</td>
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<td>Load Imbalance</td>
<td>1:00-1:20</td>
<td>Fan Guo, Kyung-Ah Sohn</td>
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Day 2: Thursday, October 11, 2007

Cache Organization and Performance for Chip Multiprocessors: How should the design of the cache hierarchy change for a chip multiprocessor?


On-Chip Interconnects: How should the on-chip interconnect be designed for a chip multiprocessor, and how does this design interact with the on-chip cache hierarchy?


Cache Coherence: Recent innovations in cache coherence protocols.


Memory Consistency: Recent innovations in supporting memory consistency models.

Table 2: Day 2 Discussion Leaders

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<thead>
<tr>
<th>Topic</th>
<th>Time Slot</th>
<th>Discussion Leaders</th>
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<tbody>
<tr>
<td>Caches for CMPs</td>
<td>12:00-12:20</td>
<td>Wittawat Tantisiriroj, Eric Blais</td>
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<tr>
<td>On-Chip Interconnects</td>
<td>12:20-12:40</td>
<td>Michael Papamichael, Hormoz Zarnini</td>
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<td>Cache Coherence</td>
<td>12:40-1:00</td>
<td>Carsten Varming, Michael Ashley-Rollman</td>
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<td>Memory Consistency</td>
<td>1:00-1:20</td>
<td>Shobhit Dayal, Dilip Kumar Uppugandla</td>
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Day 3: Tuesday, October 16, 2007

Data Parallelism: Streams and Graphics Processors: Interesting ways to exploit data parallelism for stream programs and for GPUs.


Recording Inter-Thread Data Dependencies for Deterministic Replay: To support debugging of parallel programs, we need to be able to reconstruct inter-thread data dependencies. How do we do this efficiently?


Dynamic Checking of Program Invariants: Techniques for monitoring programs as they execute to check for bugs and security problems.


**Optimizing Power and Heat:** Power and thermal issues are major constraints on hardware technology these days. What can we do to improve power efficiency?


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<tr>
<td>Data Parallelism</td>
<td>12:00-12:20</td>
<td>Yongjun Jeon</td>
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<td>Wei Yu</td>
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<td>Deterministic Replay</td>
<td>12:20-12:40</td>
<td>Jason Franklin</td>
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<td>Michelle Goodstein</td>
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<td>Dynamic Checking</td>
<td>12:40-1:00</td>
<td>Pongsin Poosankam</td>
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<td>Amar Phanishayee</td>
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<td>Optimizing Power</td>
<td>1:00-1:20</td>
<td>Karthik Lakshmanan</td>
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<td>Wenjie Fu</td>
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