

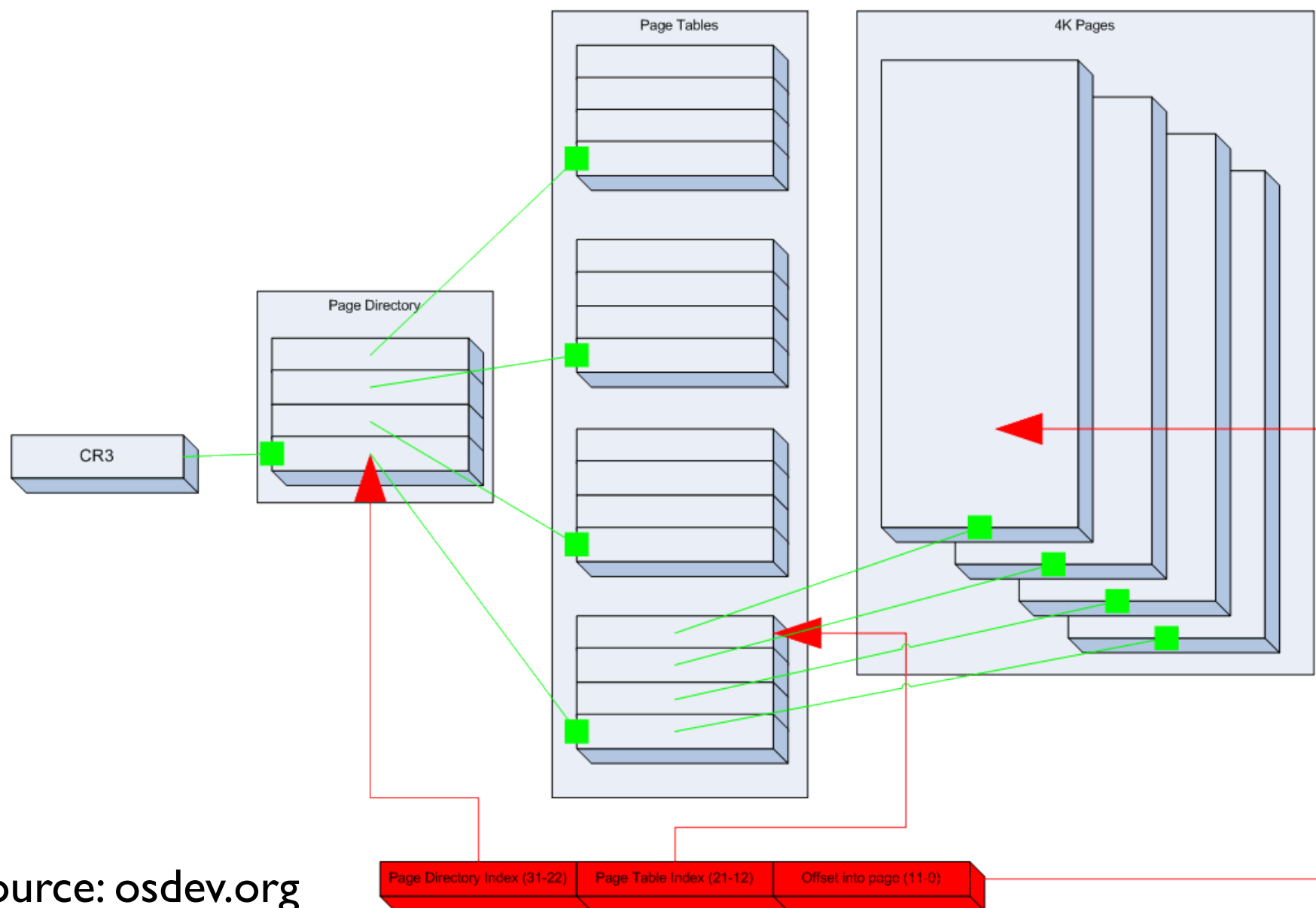
Final Exam Prep Session

Virtual Memory

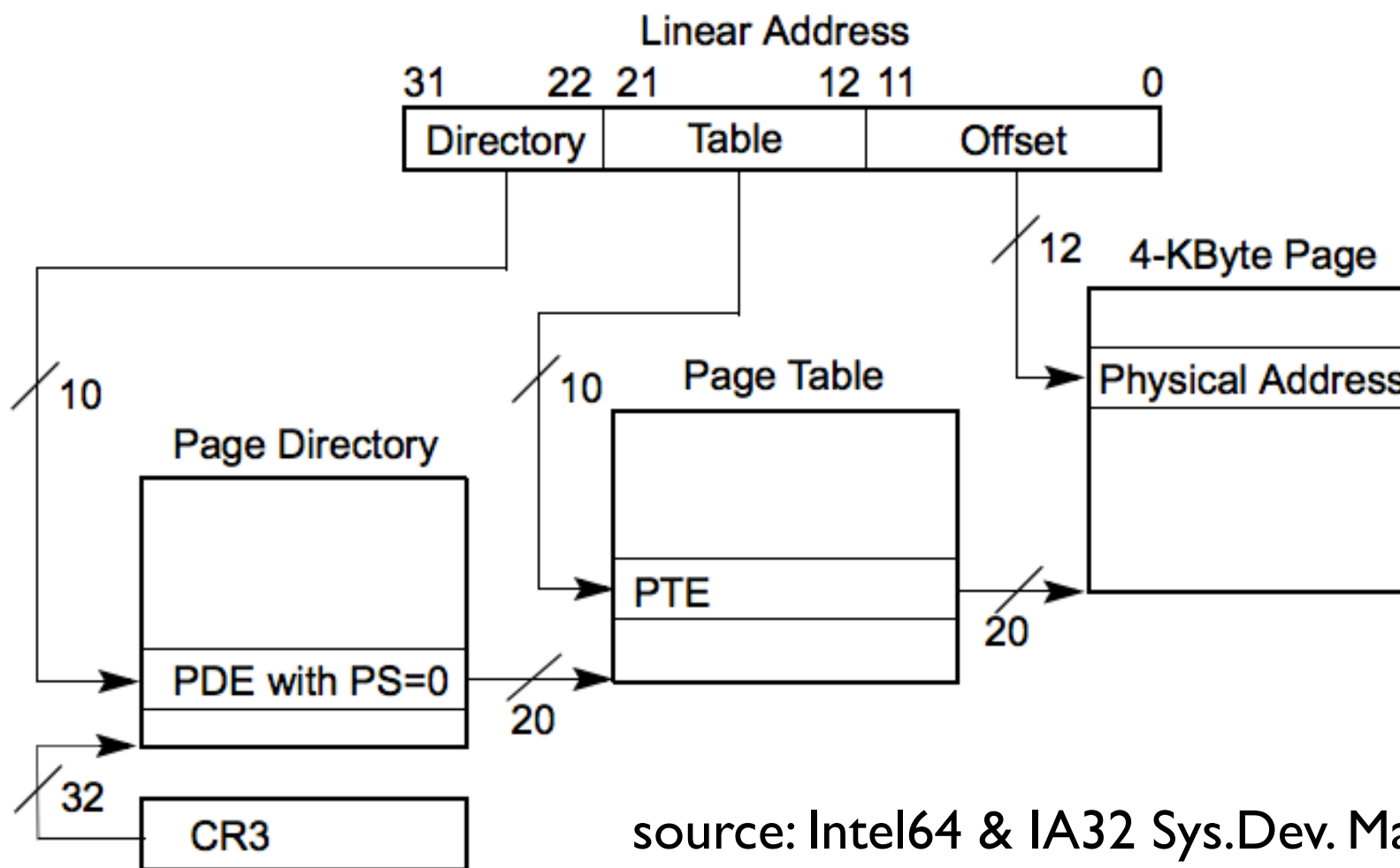
15-213: Introduction to Computer Systems
May 8, 2013

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Section C

IA32 Two-Level Page Tables



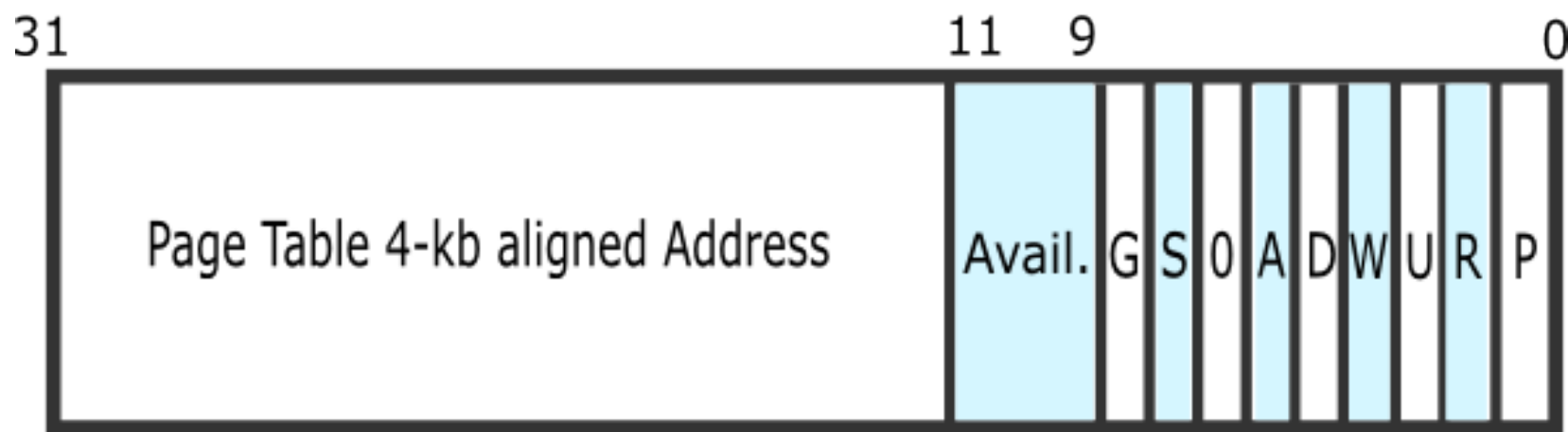
IA32 Two-Level Page Tables



source: Intel64 & IA32 Sys.Dev. Manual
Figure 4-2

IA32 Two-Level Page Tables: PDE Flags

Page Directory Entry

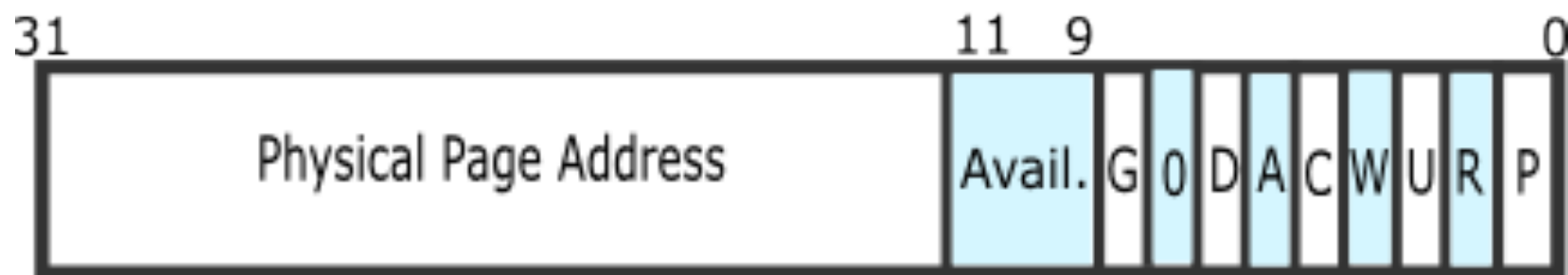


G - Ignored
S - Page Size (0 for 4kb)
A - Accessed
D - Cache Disabled
W - Write Through
U - User\Supervisor
R - Read\Write
P - Present

source: osdev.org

IA32 Two-Level Page Tables: PTE Flags

Page Table Entry



G - Global
D - Dirty
A - Accessed
C - Cache Disabled
W - Write Through
U - User\Supervisor
R - Read\Write
P - Present

TLB Lookup

VA = 0x9fd28c10 = VPN:VP0 = 9fd28c10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

VA = 0x9fd28c10 = TLBT:TLBI:VP0

TLBT = 10 0111 1111 0100 1010 = 0x27f4a

TLBI = 00 = 0x0

MISS₆

Page Directory Entry Lookup

VA = 0x9fd28c10 = **PDI** | **PTI** | VP0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

$$\begin{aligned}
 \text{phaddr(PDE)} &= \text{base(PD)} + \text{offset(PDE)} \\
 &= \text{base(PD)} + \text{PDI} * \text{sizeof(PDE)} \\
 &= \text{base(PD)} + \text{PDI} * 4 \\
 &= \text{base(PD)} + \text{PDI} \ll 2
 \end{aligned}$$

$$\text{PDI} = 10\ 0111\ 1111 = \text{27f}$$

$$\text{offset(PDE)} = \text{PDI} \ll 2 = 1001\ 1111\ 1100 = \text{9fc}$$

$$\text{phaddr(PDE)} = 0045d000 + 9fc = 0045d9fc \quad (1b)$$

PDE contents

`phaddr(PDE) = 0045d9fc`

`contents(PDE) = 0df2a237` → present bit set

`base(PT) = contents(PDE) & ~fff = 0df2a000`

Page Table Entry Lookup

VA = 0x9fd28c10 = **PDI** | **PTI** | VP0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

$$\begin{aligned}
 \text{phaddr(PTE)} &= \text{base(PT)} + \text{offset(PTE)} \\
 &= \text{base(PT)} + \text{PTI} * \text{sizeof(PTE)} \\
 &= \text{base(PT)} + \text{PTI} * 4 \\
 &= \text{base(PT)} + \text{PTI} \ll 2
 \end{aligned}$$

PTI = 01 0010 1000 = ...

offset(PTE) = **PTI** << 2 = 0100 1010 0000 = 4a0

phaddr(PTE) = 0df2a000 + 4a0 = 0df2a4a0 (1c)

PTE contents

phaddr(PTE) = 0df2a4a0

contents(PTE) = 00324236 → present bit NOT set

Page Fault

Again...



TLB Lookup

$$VA = 0x0d4182c0 = \text{VPN:VP0} = 0d418:2c0$$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0												

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0												

$$VA = 0x0d4182c0 = \text{TLBT:TLBI:VP0}$$

$$\text{TLBT} = 00\ 0011\ 0101\ 0000\ 0110 = 0x03506$$

$$\text{TLBI} = 00 = 0x0$$

TLB Contents

Index	Tag	PPN	Valid
0x0	0x03506	0x98f8a	1 (YES)



TLBI



TLBT

PA = PPN:PP0 = PPN:VP0 = 0x98f8a2c0

Again...



TLB Lookup

$$VA = 0x0a32fcd0 = \text{VPN:VP0} = 0a32fcd0$$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1												

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1												

$$VA = 0x0a32fcd0 = \text{TLBT:TLBI:VP0}$$

$$\text{TLBT} = 00\ 0010\ 1000\ 1100\ 1011 = 0x028cb$$

$$\text{TLBI} = 11 = 0x3$$

MISS

Page Directory Entry Lookup

VA = 0x0a32fcd0 = **PDI** | **PTI** | VP0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1												

$$\begin{aligned}
 \text{phaddr(PDE)} &= \text{base(PD)} + \text{offset(PDE)} \\
 &= \text{base(PD)} + \text{PDI} * \text{sizeof(PDE)} \\
 &= \text{base(PD)} + \text{PDI} * 4 \\
 &= \text{base(PD)} + \text{PDI} \ll 2
 \end{aligned}$$

PDI = 0000101000 = ...

offset(PDE) = **PDI** << 2 = 0000 1010 0000 = 0a0

phaddr(PDE) = 0045d000 + 0a0 = 0045d0a0 (3b)

PDE contents

`phaddr(PDE) = 0045d0a0`

`contents(PDE) = 000c3297` → present bit set

`base(PT) = contents(PDE) & ~fff = 000c3000`

Page Table Entry Lookup

VA = 0x0a32fcd0 = **PDI** | **PTI** | VP0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1												

$$\begin{aligned}
 \text{phaddr(PTE)} &= \text{base(PT)} + \text{offset(PTE)} \\
 &= \text{base(PT)} + \text{PTI} * \text{sizeof(PTE)} \\
 &= \text{base(PT)} + \text{PTI} * 4 \\
 &= \text{base(PT)} + \text{PTI} \ll 2
 \end{aligned}$$

PTI = 1100101111 = ...

offset(PTE) = **PTI** << 2 = 1100 1011 1100 = cbc

phaddr(PTE) = 000c3000 + cbc = 000c3cbc (3c)

PTE contents

phaddr(PTE) = 000c3cbc

contents(PTE) = 34abd237 → present bit set

contents(PTE) = PPN:flags = 34abd:237

PPN = 34abd

PP0 = VP0 = cd0

PA = PPN:PP0 = 34abdc00 (3d)

SUCCESS

PTE contents

phaddr(PTE) = 000c3cbc

contents(PTE) = 34abd237 → present bit **set**

contents(PTE) = PPN:flags = 34abd:237

base(P) = contents(PTE) & ~fff = PPN:000

PA = base(P) + offset = 34abd000 + cd0

PA = 34abdc00

What are you trying to tell me?

- That I can dodge bullets?



When you are ready

- You won't have to...

