Classical Control for Quantum Computers

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Quantum Computing is Hard

- Qubit decoherence
  - Physical isolation from environment
  - Error correction correcting error correction!
  - Decoherence-free subspaces

Quantum Computing is Harder!

- Complex physical interactions = complex pulse sequences
- Nanoscale geometries
  - Atomic interactions on the order of 10nm
- Cold operating temperatures
  - 1 Kelvin reduces thermal noise
- These issues make control circuitry difficult!
- Must account for in QC design

Skinner-Kane Si based computer

- Silicon substrate
- Qubit = phosphorus ion spin + donor electron spin
  - A-gate
    - Hyperfine interaction
    - Electron-ion spin swap
- S-gate
  - Electron shuttling
- Global magnetic field
  - Spin precession
  - Universal set of gates
Quantum wires

- Ions are stationary
  - Qubits are moved by swapping
- Alternating swap gives us “wires”
  - Some qubits move right, some left
- Quantum wires seem more complicated than classical...

Swap cell

- A lot of steps for two qubits!

Swap Cell Control

- What a mess! Long pulse sequence...

Pulse Sequence for 2-D

- 2-D layout (mentioned in Kane '00) moves electrons in parallel
  - Simpler control
  - Better electron separation
- Control signals still complicated!
  - S-gate cascade
  - A-gate sequence
**Pulse Characteristics**

- **Clock rate**
  - Electron-ion interaction period: 88.3ps -> 11.3GHz clock rate
- **Voltage swing**
  - Slower qubit manipulation
  - Lower voltage swing = lower voltage differential
- **Slew rate**
  - A-/S-gates must charge in clock period

**Qubit layout**

- Voltage swing ($V_{max}$) adjusts $d_{qubit}$
  - Tuned for desired error rate
- Slew rate and clock period adjusts $d_{Si}$
  - Lowers electrode to back gate capacitance
- Other technologies? (SOI)
- Pulse characteristics effect quantum datapath

**Single-electron transistors (SETs)**

- CMOS does not work at 1K operating temperature
- SETs work well at low temperatures
- Electrons move 1-by-1 through tunnel junction onto quantum dot and out other side
- Low drive current (~5nA) and voltage swing (~40mV)
  - Affects our error and slew rates

**Swap control circuit**

- S-/A-gate pulse sequences complex
- What would a circuit schematic look like?
Swap control circuit II

- 5-bit counter
- Reset
- Enable
- 8-bit counter
- Reset
- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 0
- D
- D
- D
- D
- D
- D
- D
- D
- D
- S1a
- S1b
- S1c
- S1d
- S2a
- S2b
- S3a
- S3b
- S3c
- S3d
- S4a
- S4b
- A
- A
- S1
- S2
- S3
- S4

A-gate pulse repeats 24 times
Off-on A-gate pulse subsequence (2 off, 254 on)

• Can this even be built with SETs?

Large!

- Control circuit area, ~10um²
  - Aggressive process, 30nm feature size
  - Minimal design
- Swap cell area, ~0.068um²
  - Will not fit!

In SIMD we trust?

- Large control circuit/small swap cell ratio = SIMD
- Like clock distribution network
- Clock skew at 11.3GHz?
- Error correction?

Why on-chip?

- Why not run many wires in from outside?
- Error correction complicates
  - Requires conditional swapping

1000 qubits
* 4 signals/qubit in swap
* 336 swaps/lvl 1 ECC
  = 1344000 wires!

• ECC could mean trouble for SIMD in general
Conclusions

• Pulse sequences for quantum gates are complex!
• All quantum computing technologies require complex pulse sequences
• Must keep control circuit in mind for large-scale integration