Enabling Nanocomputing: Opportunities for Computer Science

John N. Randall Ph.D.  V.P. Research, CTO - Zyvex Corp.

Outline

• My definition of Nanocomputing
• Bending Moore’s Law
• After CMOS: what?
• Some opportunities
• Quantum Computing

Nanocomputing

• We don’t have to wait long for Nanocomputing.
  — Sub 100nm Poly gates in production.
  — Several hundred DRAM cells in area of Red Blood cell.
  — 2GHz processors in commodity market.

• It’s already here.

• It’s called CMOS

Will CMOS die in 10 years?

• Over the past 20 years, many experts have been asked to predict the end of downscaling (and therefore the end of CMOS). I have developed a simple algorithm to determine his or her answer:

  \[
  \text{Year CMOS dies} = (\text{Year question is asked}) + 10
  \]

Opportunity #1

Massively parallel processors

• Current drive, interconnect delay, and other issues will favor arrays of smaller processors over a few mega-processors.

• Operating systems and algorithms that can parallelize general computing problems will play a major role in increasing computational power.

• Parallelism will pay dividends later.
Opportunity #2
Fault Tolerance / Error Correction
- Soft errors (Cosmic Rays), low voltages, manufacturing tolerances, etc. will all drive down circuit reliability.
- This will become a growing issue in CMOS and will certainly be an issue for other nanocomputing technologies.
- Fault tolerant and error correcting algorithms and or architectures will be essential.

Opportunity #3
Multi – Level Logic (speculative)
- Binary has been beaten to (near) death.
- Multi-valued logic allows one to do more with a given number of devices.
- Redundant Digit Logic:
  \[ 10011010111001101010011001001011 \]
  \[ +01100100101110011010111001101010 \]
  \[ 111111111010000001010010110101 \]

Redundant Digit Adder
- Base 2 Radix 4
- \[ 1 \times 16 + 2 \times 8 + 2 \times 4 + 1 \times 2 + 0 \times 1 = 42 \]
Replacing CMOS?

The Contenders

- GaAs, InP, SiC, GaN or other semiconductors of the future.
- Resonant tunneling devices
- Single Electron Transistors
- Nanotube memory devices
- Nanotube transistors
- Computing with DNA
- Molecular electronics

— The industry is littered with failed efforts to produce useful circuits with two terminal devices.

Universal 3-Input Cell

Opportunity ??

- R. A. Short (1965)
- Given Independent 3-Input functions F & G, this architecture has been shown to be functionally complete.
- However, no general design approach was developed.

Vertical Rail Cellular Cascade

Quantum Computing

- A distinctly new paradigm in computation.
- Using coupled quantum states it has been demonstrated that intermediate superposition of states can carry enormously more information than is possible with a classical computer.
- Several implementations are being pursued, including Si solid state devices.

Classical Bit vs. Quantum Qubit

<table>
<thead>
<tr>
<th>Classical Bit</th>
<th>Quantum Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 = &lt;i&gt; \uparrow \leftrightarrow \downarrow \rangle =</td>
<td>0\rangle</td>
</tr>
<tr>
<td>1 = &lt;i&gt; \uparrow \downarrow \rangle</td>
<td>1 = \langle 1</td>
</tr>
</tbody>
</table>

Quantum Bit is any two-level quantum system, for example, Electron Spin

\[ \text{It's an error!} \quad \text{It's a superposition!} \]
Quantum Computing

The BIG Deal

- The electronics industry has managed 3 decades of exponential growth in computing power mainly because a linear decrease in L produces a \((1/L)^2\) increase in devices.
- With a classical approach, computational power increases linearly with the number of devices.
- With quantum computing, computational power goes up exponentially with the number of devices.

Opportunity #4

- So far only a few algorithms (Shor’s & Grover’s) have been demonstrated as very efficient QC algorithms.
- Get to know a physicist.
Moore’s-curve

- Gate Length [nm]
- Date

Tunneling Limits Gate Oxide

- Gate Voltage (V)
- Current (A/cm²)

Worst Case Scenario*

- Computer Scientists fail to develop FTA
- Semiconductor yields crash
- Electronics industry stagnates
- Consumers stop spending

* P. Ware & M. Levenson,
Worst Case Scenario

- Semiconductor yields crash
- Electronics industry stagnates
- Consumers stop spending
- Computer Scientists fail to develop FTA
- Hyperinflation
- Mass unemployment
- Economy collapses
- Starvation

*P. Ware & M. Levenson, Semicon West 1998

Two spins:

Four states in superposition: $2^2$

$|00\rangle + |01\rangle + |10\rangle + |11\rangle$

Entanglement of spins 1 and 2

N spins:

$2^N$ states in superposition

$|00\rangle + |01\rangle + \ldots + |1\rangle + \ldots + |1\rangle$