DEVICE AND CIRCUIT OPTIONS FOR SUB-10-NM ELECTRONICS

Konstantin K. Likharev
Stony Brook University, Stony Brook, NY
klikharev@sunysb.edu

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CMOS TECHNOLOGY

Intel’s Pentium 4 processor (2000):
• 42 million transistors
• 1.4 GHz clock frequency (now up to 2.53 GHz)

ITRS
INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
2001 EDITION

10-NM-SCALE MOSFET: A BULK ELECTRODE MODEL

Features:
• 2D Poisson solver
• source to drain tunneling (WKB approximation)

SOURCE-DRAIN I-V CURVES

L = 10 nm
L = 5 nm
\( t_{ox} = 1.5 \text{ nm}, \ t = 2 \text{ nm}, \ N_d = 3 \times 10^{20} \text{ cm}^{-3} \)

SUBTHRESHOLD CURVES

V = 0.3 V
60 mV/dec
0.6 V
V = 0.3 V
0.0 V
V/16
V/16
Carnegie Mellon U., October 2002

VOLTAGE GAIN (DIBL-1)

\[ V = 0.3 \text{ V}, \quad t_{ox} = 1.5 \text{ nm}, \quad t = 2 \text{ nm}, \quad N_D = 3 \times 10^{20} \text{ cm}^{-3} \]

V = 0.3 V, \( t_{ox} \) = 1.5 nm, \( t \) = 2 nm, \( N_D \) = 3 \times 10^{20} cm^{-3}

PROBLEM #1: POWER SCALING

51 0 1 5 2 0

0 10 20 30 40 50

Voltage Gain

\[ G \]

Gate Length

\[ L \]

L = 12.5 nm

10 nm

7.5 nm

5 nm

2.5 nm

(!!!)

PROBLEM #2: FAB SENSITIVITY

5 0 1 5 2 0

0 10 20 30 40 50

Voltage Gain

\[ G \]

Gate Length

\[ L \]

L = 12.5 nm

10 nm

7.5 nm

5 nm

2.5 nm

1 nm

0.1

100 mV

Main advantage:

- low surface scattering

at nm channel width

Main problems:

- electrode contacts
- chirality control

CARBON NANOTUBE TRANSISTORS: A PANACEA?

Main advantage:

- low surface scattering

at nm channel width

Main problems:

- electrode contacts
- chirality control

SET vs FET

Choice:

\[ G \leftrightarrow \theta^2/\theta \]

quantum \( \rightarrow \) FET \( \leftrightarrow \) SET \( \leftrightarrow \) classical

Yu. Pashkin et al., APL 76, 2256 (2002)

SINGLE-ELECTRON TRANSISTOR

- Averin and Likharev, 1985 (theory)
- Fulton and Dickey, 1987 (AMC)
- Oosterbaan et al., 1993 (GaAs/AlGaAs)
- Monot et al., 1993 (GaAs/AlGaAs)
- ...
SET LOGIC FAMILY
(R. Chen et al., 1995-96)

NOR/NAND

NOT               XOR

A \rightarrow A + B
B

A

A

A \rightarrow A \oplus B

A

A

A

PROBLEM #1: FABRICATION

Island Capacitance (F)

Island Diameter (nm)

0.1 1 10 100 1000

10^{-3}

0.01

0.1

1

10

10^{-16}

10^{-17}

10^{-18}

10^{-19}

Energy (eV)

Ek

Ec

Ea

1-nm-SCALE DEVICE FABRICATION

"Quantum Coral" (IBM-Almaden, early 1990s) Radius 7.1 nm

PROBLEM #2:
RANDOM BACKGROUND CHARGE

A single charged impurity...

...is sufficient to shift the Coulomb blockade threshold

see also:
- E. S. Solntsov et al. (MSU)
  JETP Lett. 64, 556 (1996)
- N. Zhitenev, H. Meng, and Z. Bao
  PRB 88, 226801 (2002)

J. Park et al. (Cornell U.)
HYBRID SET/FET MEMORIES:

two options

dynamic (destructive) readout (K.L. & A. Korotkov, 1995)
background charge compensation (A. Korotkov, 2001)

word line
(crested) tunnel barrier
floating

gate
bit
line +
bit
line -
SET
island
next cell

HYBRID SET/FET MEMORIES:

two options

MEMORY SCALING COMPARISON

Other competition:
- FRAM
- MRAM
- OUM
problems below ~20 nm?

ESTOR: BASIC IDEA
(K.L. and A. Korotkov, 1995)

Features:

- 1 bit: ~20 electrons in ~30 grains
- SET/FET read-out
- Estimated density beyond 1 Tbit/in²
- Estimated bandwidth >1 Gbps

SET LATCHING SWITCH
AS BIWAS SYNAPSE
S. Fölling, Ö. Türel, and K.L., Proc. IJCNN'01, pp. 216-221

SINGLE-MOLECULE SYNAPSE CONCEPT
A. Mayr, SBU/Chemistry, unpublished

NEUROMORPHIC NETWORKS

Cerebral cortex:
~ 2 × 10¹⁰ neural cells
~ 10⁴ connectivity
⇒ ~10¹⁴ synapses
HYBRID MOLECULAR-NANOWIRE-CMOS CIRCUIT CONCEPT

FREE-GROWING NETWORKS

Legend:
- cell bodies
- growing axons
- growing dendrites
- frozen axons
- frozen dendrites
- synapses

But: poor scaling!

CROSSNET SPECIES

Δx = Δy = const = M

FlossBar:
Δx = Δy = const = M

RandBar:
Δx = Δy = const = M

InBar:
Δx = Δy = const = M

CROSSNET SYSTEM HIERARCHY

INBAR-BASED BLOCK

WORLD

CROSSNET SYSTEM HIERARCHY

SENSOR/ACTUATOR SYSTEM

I/O SYSTEM

TUTOR

HIGH SPEED BUS

CELL BLOCK

CELL BLOCK

CELL BLOCK

CELL BLOCK

SOMA

SOMA

SOMA

Flat axon - dendrite - synapse array
CROSSNET SIGNAL SIGN ANTISYMMETRY

CROSSNET TRAINING:

PROBLEMS...
- no access to individual synapse (backprop not an option)
- huge information volume (~10^5 Encyclopedia Britannica’s)

BUT:
- broadband (~10 Mbps/channel) access:
  10^9 Bytes ~ 3 × 10^9 pad-hours
- high I/O pad density (~250 pads/cm):
  ~3×10^9 pads → 1 hour upload

…and Options
- global reinforcement training
  (possibly including IC analysis):
  • semi-global training
  • global reinforcement training

CONCLUSIONS I:
DEVICES, CIRCUITS, AND SYSTEMS
- CMOS may stall at ~ 10 nm
  (depending mostly on fab economy)
- to carry on, two grand challenges:
  - chemically-assembled single-molecule devices
    (either SET or possibly FET-like)
  - new circuit / system architecture ideas
    (e.g., CrossNets)
- systems: hybridization with CMOS a must!

CROSSNET SCALING

Synaptic template area: \( A_s \sim 8 F^2 \)
for \( F \approx 2 \text{ nm, } A_s \sim 16 \times 16 \text{ nm}^2 \), density \( n_s \sim 4 \times 10^{11} \text{ cm}^{-2} \)

Cell body density:
for \( M = 10^4 \), \( n_c \sim 4 \times 10^7 \text{ cm}^{-2} \)
i.e. 2×10^18 cells & 2×10^14 synapses on 
~ 20×20 cm^2 of Si (!)

Intercell latency: \( \tau_0 \sim 10^{-7} \text{ s} \) (!!)
(cf. ~10^{-3} s in bio)

CONCLUSIONS II:
MOST URGENT CAD TOOL NEEDS
- for devices:
  - a bridge between ab initio molecular structure calculations and transport properties simulation
- for circuits:
  - molecular chemical assembly simulation tools
  (molecular dynamics)
- for systems:
  - effective NN training option study algorithms
  (cluster → grid computing?)
E.g., Njaf…
(165 processors, 72 GFLOPS Linpack)
…still, way too small!
THANK YOU!