NSF Science and engineering workshop

Nanocomputing design science challenges

George Bourianoff
Intel Corporation and Semiconductor Research Corporation
CMU Pittsburgh, Pa
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Outline

- CMOS forever
  - Scaled silicon and the ITRS
  - The foundations of scaling
  - The economics of scaling
  - CMOS device circa 2015
- Alternative technologies
  - A universe of options
  - Selection criteria
- Age of integration –CMOS + other stuff
- Conclusions

Thesis

- Conventional scaling of CMOS will end in near term (10 to 15 years)
- That will be followed by a period of heterogeneous integrations of dissimilar technologies on silicon based platforms in the intermediate term (10-20 years)
- Finally, radical new scalable information processing technologies will emerge in the far term (> 20 years)

Goal

- Define the design sciences required to integrate novel information processing technologies with existing computational infrastructure in an evolutionary manner

The beauty of silicon

For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by scaling.

<table>
<thead>
<tr>
<th>DRAMs</th>
<th>1990</th>
<th>1995</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size</td>
<td>2.5/2.3</td>
<td>2.7/2.4</td>
<td>2.9/2.5</td>
</tr>
<tr>
<td>Wafer diameter</td>
<td>6&quot;</td>
<td>6&quot;</td>
<td>12&quot;</td>
</tr>
<tr>
<td>Cost per Megabit</td>
<td>$6.50</td>
<td>$3.14</td>
<td>$0.10</td>
</tr>
</tbody>
</table>

Source: ICE

Scaling will get harder

- For the first time, scaling appears to have reached fundamental limits in several areas.
- Current ITRS contains several major barriers (“brick walls”) with no known solutions.
- Barriers are approaching fast with the acceleration of the ITRS over the past 5 years.
- Overcoming these barriers will require:
  - New materials
  - New types of devices
  - New physical models
  - New types of processing
  - New design tools & methodology

Brick Walls on the ITRS

Solution: New solution being pursued
No known solutions
The economic imperative

Material Evolution in MOS

2000's

60's

70's

80's

90's

Al

SiO₂

Al-Si

SiO₂

Poly

Al-Cu

SiO₂

Ti/TiN

W

Al-Cu

SiO₂

TiSi₂/Poly

Ti/TiN

W

Low K

SiO₂/SiN

CSi₂/Poly

Ti/TiN

W

ELK

Silicon

New materials

Improved processing

New geometries

Scaling will continue as long as \((\delta \text{ cost})/(\delta \text{ performance}) > \text{ alternate technologies}\)

CMOS device circa 2016

- **Cost**: \(10^{-11}\) $/gate
- **Size**: 8 nm / device
- **Speed**: 0.2 ps / operation
- **Energy**: \(10^{-18}\) J/operation

Alternative technologies

Emerging Technology Sequence

Emerging Technology Parametrization

Which technologies will dominate?

- Economic relevance criteria
  - The risk adjusted ROI for any new technology must exceed that of silicon
- Caution
  - Sufficiently advanced technologies will create their own applications. New technologies cannot necessarily be justified by current day applications.
Which technologies will dominate? What are the selection criteria?

- Energy efficiency
- CMOS compatibility
- Performance
- Scalability
- Architectural compatibility
- Sensitivity to parametric variation
- Room temperature operation
- Stability and reliability

Age of integration

The challenge

Changing architectural paradigms

Current

- Boolean logic
- Binary data representation
- 2D
- Homogeneous
- Globally interconnected
- Synchronous
- Von Neuman
- 3 terminal

Future

- Neural networks, CNN, QCA, ...
- Associative, patterned, memory based, ... data representations
- 3D
- Non homogeneous
- Nearest neighbor
- Asynchronous
- Integrated memory/logic
- 2 terminal

System software design needs to facilitate emerging technologies

Challenge

- CMOS is based on Boolean logic and binary data representation
- Alternative technologies will require “native” logic systems and data representations to optimize their performance

Solution?

- Design science must provide functional abstractions and interfaces to couple multiple, dissimilar technologies into a single functional system

Emerging Research Architectures
Heterogeneous 3D integration

- 3D integration
  - Shorter interconnects
  - High aerial density
  - Thermal management
  - Test and measurement
- Heterogeneous integration
  - Integration of new devices
  - Difficult interfaces
  - Manufacturing issues
  - Lack of design tools

Quantum cellular automata

- Local interconnection
  - High density
  - Self assembly
  - No interconnects in signal path
  - Limited fan out
  - Sensitive to stray charge
- Asynchronous
  - No clock signal
  - Logic complexity

Quantum Cellular Automata

Floating adder executed with Quantum Cellular Automata (U. Notre Dame)

Fault tolerant architecture

- Integration of imperfect devices
- Two terminal devices
  - Consistent with self assembly, bio technology
- Lack of gain
- Requires pre testing
- High interconnect density

Molecular architecture

- Supports new charge transport mechanisms
- Supports self assembly
- Requires memory based logic
- Primarily 2 terminal logic

Tunneling Phase Logic

- Local interconnections
- Supports RTD integration
- Non charge encoded logic and signaling
  - Electrical phase
  - Low transition energy
  - Multi-valued logic
  - Requires pump signal
- Sensitive to stray charge
Quantum computing

- Non charge encoded logic and signaling
  - Quantum phase information
- New applications
- Exponential speedups
- Secure information transmission
- Extreme sensitivity to everything

Conclusions

- Scaled CMOS will dominate microelectronics for next 15 years and provide the common platform indefinitely
- Alternative technologies will require native logic systems and data representations to be developed
- Integration and market acceptance will require functional abstraction and transparent interfaces