Dealing With Defects

- Need to discover the characteristics of the individual components, but
- Can’t selectively stimulate or probe the components
- Download test machines

Built-In Self-Test

- Configure testers vertically
- Configure testers horizontally
- Identify fault!

Configure the device to test itself!

Reconfigurable Computing

- General-Purpose
- Custom Hardware
- General-Purpose Custom Hardware

Logic Blocks
Routing Resources

Advantages of Reconfigurable

- Flexibility of a processor
- Performance of custom hardware
- Defect Tolerant

Heart of an FPGA

The cost of the FPGA:
Increased Area-Delay Product

Universal gate = RAM

Switch controlled by a 1-bit RAM cell
Heart of an FPGA

The cost of the FPGA: Increased Area-Delay Product

- RAM cell
- Wires to program RAM cell

Switch controlled by a 1-bit RAM cell

The cost of the FPGA:

- RAM cell
- Wires to program RAM cell

Switch controlled by a 1-bit RAM cell

Key Component: Reconfigurable Switch

http://www.chem.ucla.edu/dept/Faculty/stoddart/research/mv.htm
Key Component: Reconfigurable Switch

- Holds its own configuration state
- Can be programmed with the signal wires

Wires
- Small (≥ 2nm)
- Long (≤ 3000nm)
- Excellent conductors
- Examples:
  - Carbon nanotubes
  - Silicon nanowires
  - Functional wires

Devices
- What you would expect:
  - Resistors
  - Diodes
  - Negative Differential Resistors (NDRs)
  - Transistors
  - Reconfigurable Switches
- Molecules are "easily" engineered
  - E.g., Diodes with 0.1V turn-on
  - MANY MANY possible molecules

What Can We Expect?
- ≥ 10^{10} gate-equivalents/cm²
- ≤ 1 Watt/cm²
- ≤ nanocents per gate
- ≥ 10^{11} ops/sec
- High defect densities

Fabrication Is Different!
- Electronic nanotechnology separates:
  - Manufacturing of devices
  - Fabrication of the circuit
- Manufacture wires and devices
- Somehow glue them together
- Assembly, Assembly, Assembly

Parallel Wires
- Can align wires
- Can mix types of wires
- Not precise
Diode-resistor Logic

Configured “ON”

Configured “OFF”

Nano-implementation

Half adder

A
B
S = A ⊕ B
C = A ^ B

NanoBlock

Diode-matrix

Molecular-latches

Stripped regions indicate connections from the CMOS layer.

NanoBlock

SE
Intra-cluster routing

Cluster of NanoBlocks

The NanoFabric

- Nanoscale layer put deterministically on top of CMOS
- Highly regular
- ~10^8 long lines
- ~10^6 clusters
  - Cluster has 128 blocks

Area (10^6 units/cm^2 available)

Typical Program Graph (g721_e)

Memory reads

Control flow transfer

100% memory cluster

100% code cluster

Typical Program Graph (g721_e)

Memory reads

Control flow transfer

memory

memcpy
Program Graph After Inlining memcpy