

Yirng-An Chen

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EDUCATION

Carnegie Mellon University, Pittsburgh, Pennsylvania, USA.

Ph.D. (Computer Science), June, 1998.

Thesis: *Arithmetic Circuit Verification Based on Word-Level Decision Diagrams*

Thesis Committee: Randal E. Bryant (Chair), Edmund M. Clarke, Rob. A. Rutenbar, Xudong Zhao (Intel).

National Tsing-Hua University, Hsin-Chu, Taiwan Republic of China.

M.S. (Computer Science), June, 1989.

Thesis: Two Global Routers.

Advised by Prof. Youn-Long Lin.

TungHai University, Tai-Chung, Taiwan, Republic of China.

B.S. (Computer Science), June, 1987.

ACADEMIC AWARDS

2003: Best paper award of 2003 IEEE CAD Transactions Best Paper Award.

1995: Best paper award of 32nd Design Automation Conference.

1992-1998: Graduate Fellowship, Carnegie Mellon University.

PRODUCT AWARDS

2003: Verdi: EDN 2002 Innovation of the Year Awards Finalist.

2005: Verdi: DesignVision Awards by International Engineering Consortium.

2005: Magellan: DesignVision Awards by International Engineering Consortium.

WORK & RESEARCH EXPERIENCE

Synopsys Inc., Mountain View, CA, Sr. Staff Engineer.

(October 2003 - Present) Working on a formal verification product named Magellan. Improving its performance and capacity by improving modeling and formal verification techniques. Filed a patent in February 2005. (October 2003 - Present)

Novas Software Inc., San Jose, CA, Technical Director.

Co-plan a series of products. Co-architect and co-implement the first product, Verdi, named EDN 2002 Innovation of the Year Awards Finalist. Architect and lead the team to develop the second product. (January 2001 - October 2003)

National Chiao Tung University, Hsinchu, Taiwan, Assistant Professor.

Teaching Computer Architecture and Formal Verification classes. Developing formal verification system for both control-path and data-path circuits. (August 1998 - January 2001)

Motorola's Advance System Tool Lab., Austin, USA, Visiting Researcher.

Developed Motorola's formal verification tool. (June 1998- August 1998).

Carnegie Mellon University, Pittsburgh, PA, USA. Ph.D. Student.

Developed Binary Moment Diagrams (BMDs) to represent integer functions effectively. Applied BMDs to the verification of integer arithmetic circuits including integer multipliers and dividers. Created Multiplicative Power Hybrid Decision Diagram (*PHDD) to represent floating point functions effectively. Improved Word-Level SMV with *PHDD and conditional forward simulation. Proved the correctness of the floating point adder in an Intel processor using improved Word-Level SMV. Found bugs in the floating point adder from University of Michigan using improved Word-Level SMV. Applied Binary Decision Diagrams to design rule checking. (August 1992 - May, 1998).

Intel's Strategic CAD Lab, Portland, Oregon, USA. Summer intern.

Developed the next generation of Intel's formal verification tool. Provided consulting service to verification engineers on formal verification. (Summer 1997).

Intel Development Lab, Portland, Oregon, USA. Summer Intern.

Verified arithmetic circuits in an Intel processor using Word-Level SMV. Suggested improvements of Word-Level SMV. (Summer 1995). Developed Intel's formal verification tool. Verified several arithmetic circuits which can not be verified by designers. (Summer 1996).

Telecommunications Laboratory of the Telecommunications Bureau, Tao-Yuan, Taiwan, Republic of China. Assistant Researcher.

Designed system architecture and function blocks of CCS network OA&M. Evaluated cost-efficiency of the model. (June 1991 - July 1992).

Military, Taiwan, Republic of China.

Mandatory military service. (July 1989 - May 1991).

National Tsing-Hua University, Taiwan, Republic of China. Research Assistant.

Developed two global routers, supervised by Prof. Youn-Long Lin. (June 1988 - June 1989). Designed VLSI chip for image processing. supervised by Prof. Long-Wen Chang. (August 1987 - June 1988).

PUBLICATIONS

Yu-Chin Hsu, Bassam Tabbara, Yirng-An Chen, Furshing Tsai, "Advanced Techniques for RTL Debugging", In 40th Design Automation Conference, Jun. 2003.

Yirng-An Chen, Fang-Sung Chen, "Algorithms for Compacting Error Traces", in Proceeding of Asian-Pacific Design Automation Conference ASPDAC '01, Jan., 2003.

Yirng-An Chen, Randal E. Bryant, “ An Efficient Graph Representation for Arithmetic Circuit Verification”, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001.

Chien-Pang Lu, Wen-Chien Liu, Yirng-An Chen, “High Probability High DENSITY State Traversal”, In IEEE 10th International Workshop on Logic & Synthesis, June, 2001.

Randal E. Bryant, Yirng-An Chen, “Verification of Arithmetic Circuits Using Binary Moment Diagrams,”, in International Journal on Software Tools for Technology Transfer, 2001.

Jiunn-Chern Chen, Yirng-An Chen, “Equivalence Checking of Integer Multipliers”, In Proceeding of Asian-Pacific Design Automation Conference ASPDAC '01, Jan., 2001.

Yirng-An Chen, Randal E. Bryant “Verification of Floating Point Adders,” Proceeding of 10th International Conference of Computer Aided Verification, pp.488-499, June 28 - July 2, 1998

Bwolen Yang, Yirng-An Chen, Randal E. Bryant and david R. O'Hallron, “Space- and Time-Efficient BDD Construction via Working Set Control”, In Proceeding of Asian-Pacific Design Automation Conference ASPDAC '98, Feb., 1998, pp. 423-432.

Yirng-An Chen, Randal E. Bryant, “*PHDD: An Efficient Graph Representation for Floating Point Circuit Verification,” In Proceedings of International Conference of Computer-Aided Design, Nov. 1997, pp. 2-7.

Yirng-An Chen, Randal E. Bryant, “ACV: An Arithmetic Circuit Verifier,” In Proceedings of International Conference of Computer-Aided Design, Nov. 1996, pp. 361-365.

Yirng-An, Chen, E. Clark, P.-H. Ho, Y. Hoskote, T. Kam, M. Khaira, J. O'Leary, X. Zhao, “Verification of all circuits in a floating-point unit using word-level model checking,” In Proceedings of Formal Methods in Computer-Aided Design, Nov. 1996, pp.19-33.

Randal E. Bryant, Yirng-An Chen, “Verification of Arithmetic Circuits with Binary Moment Diagrams,” In 32nd Design Automation Conference, Jun. 1995, pp. 535-541.

Yirng-An Chen, Young-Long Lin, and Long-Wen Chang, "A Systolic Algorithm for the K-Nearest Neighbors Problem", In IEEE Tran. on Computers, Vol. 41, No. 1, Jan. 1992, pp.103-108.

Yirng-An Chen and Young-Long Lin, “A New Global Router for ASIC Design Based on Simulated Evolution”, In 1989 Proceedings of International Symposium on VLSI, Technology, Systems and Applications, pp.261-265.

Program Committee

Asian-Pacific Design Automation Conference ASPDAC 2000-2003

Conference Session Chair

Asian-Pacific Design Automation Conference ASPDAC 2000-2005

Reviewer

Design Automation Conference (DAC), 1997 to present

Asian-Pacific Design Automation Conference ASPDAC 2000 to present

International Conference on Computer-Aided Design (ICCAD), 1998

International Conference on Formal Methods in Computer-Aided Design (FMCAD), 1998

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998 to present

Journal of Electronic Testing, 2000.