Project Proposal for CS740: Computer Architecture

Configuration Swapping and Caching

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Project Description

Currently many researchers are exploring how a reconfigurable fabric could be integrated with a processor. Few studies have been made of configuration caching & swapping; no one has yet made a study of the effect of multitasking on such a system. One of the resources that may affect performance of a reconfigurable system in a multitasking environment is the configuration cache of the reconfigurable functional unit(RFU). A study of the behavior of programs in such an environment may provide a good insight to manage the configuration cache efficiently and design a high performance reconfigurable system that can be interfaced to a general-purpose microprocessor. In this project we will study the behavior of applications in reconfigurable system and explore how to manage the configuration cache in and between the applications.

Plan of Attack

1. Analyze C code (*a*) from Mediabench, SPEC CPU95 and extract functions that can be implemented on the reconfigurable function units (*b)*. We plan to do this part using *find_custom* tool that extracts RFU-implementable functions from C code. This tool is part of the SUIF/Impact simulation suite from the PipeRench group at CMU.
2. Compile the generated rfuOp functions and benchmark code to generate instrumented binaries (*c*) used for detailed simulation and performance study of configuration sizes. Get detailed simulation results for various RFU implementation parameters (input and output ports, latency, size, speed) (*d*).
3. Perform a study of the configuration sizes for the RFU. What are the configuration sizes, how often is the RFU used, how often will configurations need to be swapped in/out for new operations - a caching analysis study (*e)*. Organize results (*f).*
4. Study of multitasking and its effect on configuration caching (past research)(*g)*, modelling configuration caching and swapping in a multitasking environment (*h)* and analysis of behavior (*i).* Organize all results(*j)*; if possible study different configuration cache replacement strategies and their effect on system performance in multitasking environment (*k)*.

Critical Path: a -> b -> c -> d -> e -> g -> h -> i -> j
Possible Additional Task: k

Probable Schedule

Week 1	Read related papers; install & get familiar with the ATOM instruction tracing tool. Get familiar with find_custom RFU extraction tool and IMPACT compiler from *Piperench* suite.
Week 2	Analyse benchmarks; extract rfu implementable sections and

generate code; compile and simulate on IMPACT; identify RFU configuration parameters and values.

Week 3 Perform cache analysis, identify frequency of caching &swapping, effect on performance. Write project milestone.

Week 4 Study behaviour of multitasking loads with respect to cache accesses. Model RFU configuration caching/swapping here.

Week 5 Generate caching performance results for multitasking behavior; collate results, write final report.

The above tasks are supposed to be done by Suraj Sudhir and Suman Nath together

Milestone

By November 8th, we should complete analysis of the configuration sizes, frequency of caching and swapping of RFU configuration data and organization of results. This will be followed in the last two weeks by the study & simulation of multitasking system loads and corresponding caching/swapping loads imposed on the RFUs, as well as its performance analysis.

Literature Search

- S.M.Scalera, J.R.Vasquez, "*Design and Implementation of a Context-Switching FPGA*" Proceedings of the IEEE symposium on FPGAs for Custom Computing Machines (FCCM) 1998.
- Z.Li, K.Compton, S.Hauck, "*Configuration Caching Management Techniques for Reconfigurable Computing*" Proceedings of the IEEE symposium on FPGAs for Custom Computing Machines (FCCM) 2000.
- K.Walker, M.Budiu, S.C.Goldstein, "*Interfacing Reconfigurable Logic with a CPU*" *Unpublished, 2000*
- C.Lee, M.Potkonjak, W.H.Mangione-Smith, "*Mediabench: a tool for evaluating and synthesizing multimedia and communications systems*" Proceedings of 30th ACM/IEEE Intl. Symposion on Microarchitecture (MICRO) '97.
- Standard Performance Evaluation Corp. *SPEC CPU95,* www.spec.org

Tools & Resources

- SUIF/Impact Reconfigurable System Simulation suite (from the *PipeRench* group in CMU)
  status: installed
  utility: *find_custom,* instrumented binary generation and compilation, simulation
- Simplescalar System Simulator
  status: installed
  utility: generic performance evaluation
- Dinero Cache Simulation Tool.
  status: installed
  utility: basic caching study
- Machines : own workstations (PIII 733 Mhz & PII 500 Mhz), Dinero will be run on the class Alphas. We estimate about 15-20 hours of usage of the Alpha machines for cache analysis. Analysis with SUIF/Impact will take roughly 50 hours. Further, study of multitasking requirements and analysis of caching in multitasking environment will take 30-35 hours.

Getting Started

We have already met Dr.Seth Goldstein for detail discussion on how the project could be implemented, and also have the SUIF/Impact infrastructure installed and running. Currently we are reading the documentation on the area. Necessary tools have been obtained and compiled on our systems.