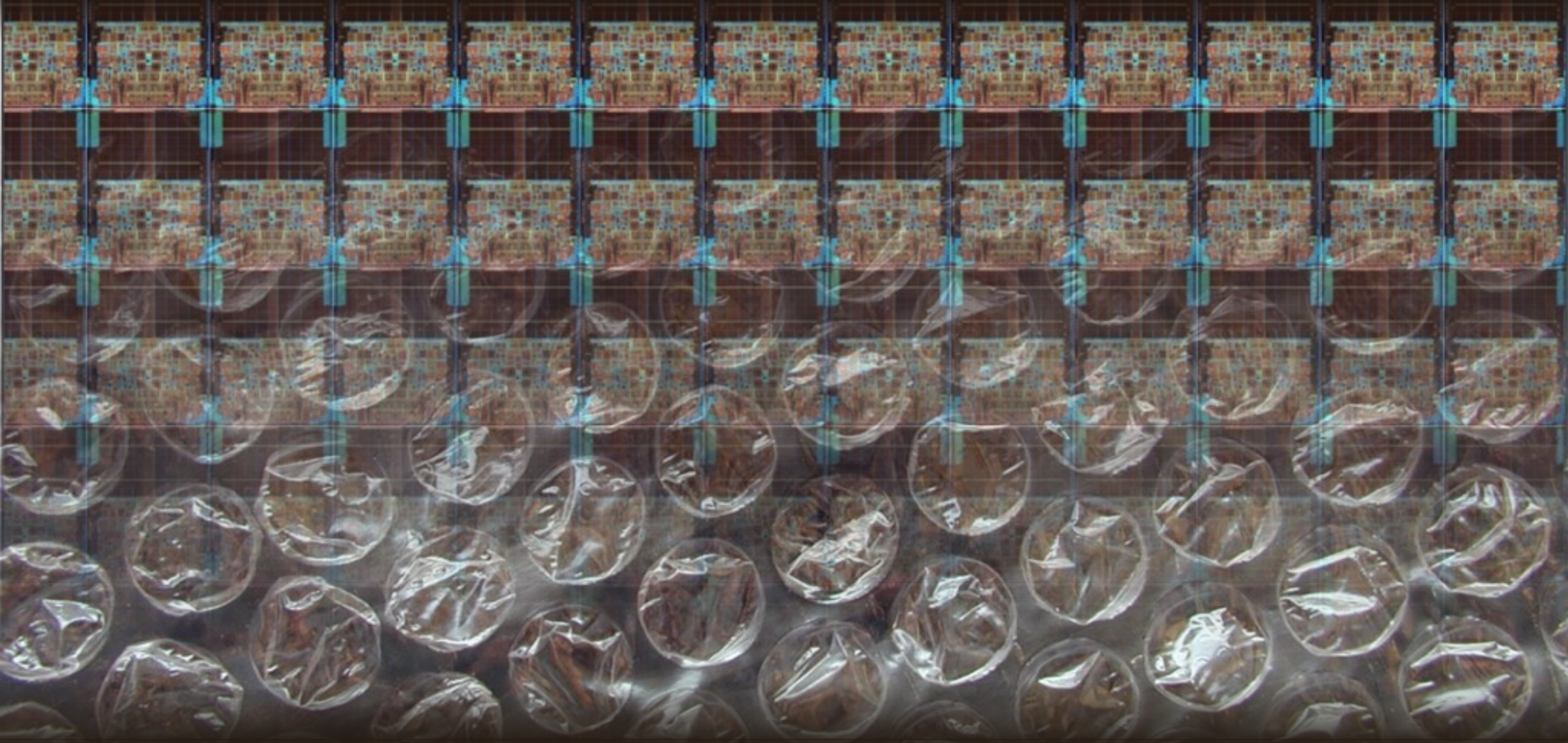
BubbleWrap: Popping CMP Cores for Sequential Acceleration



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University of Illinois

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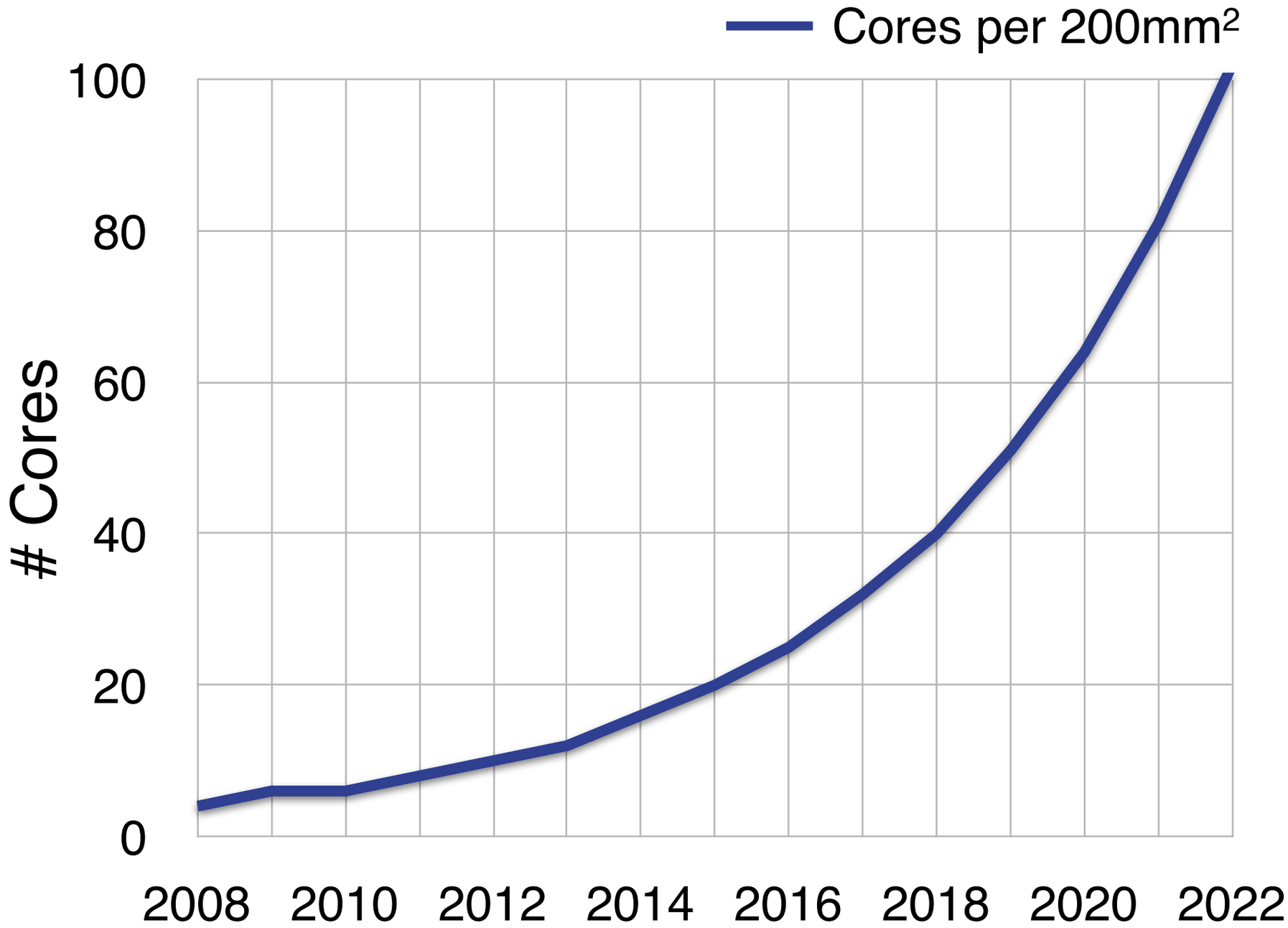
ITRS Power Scaling



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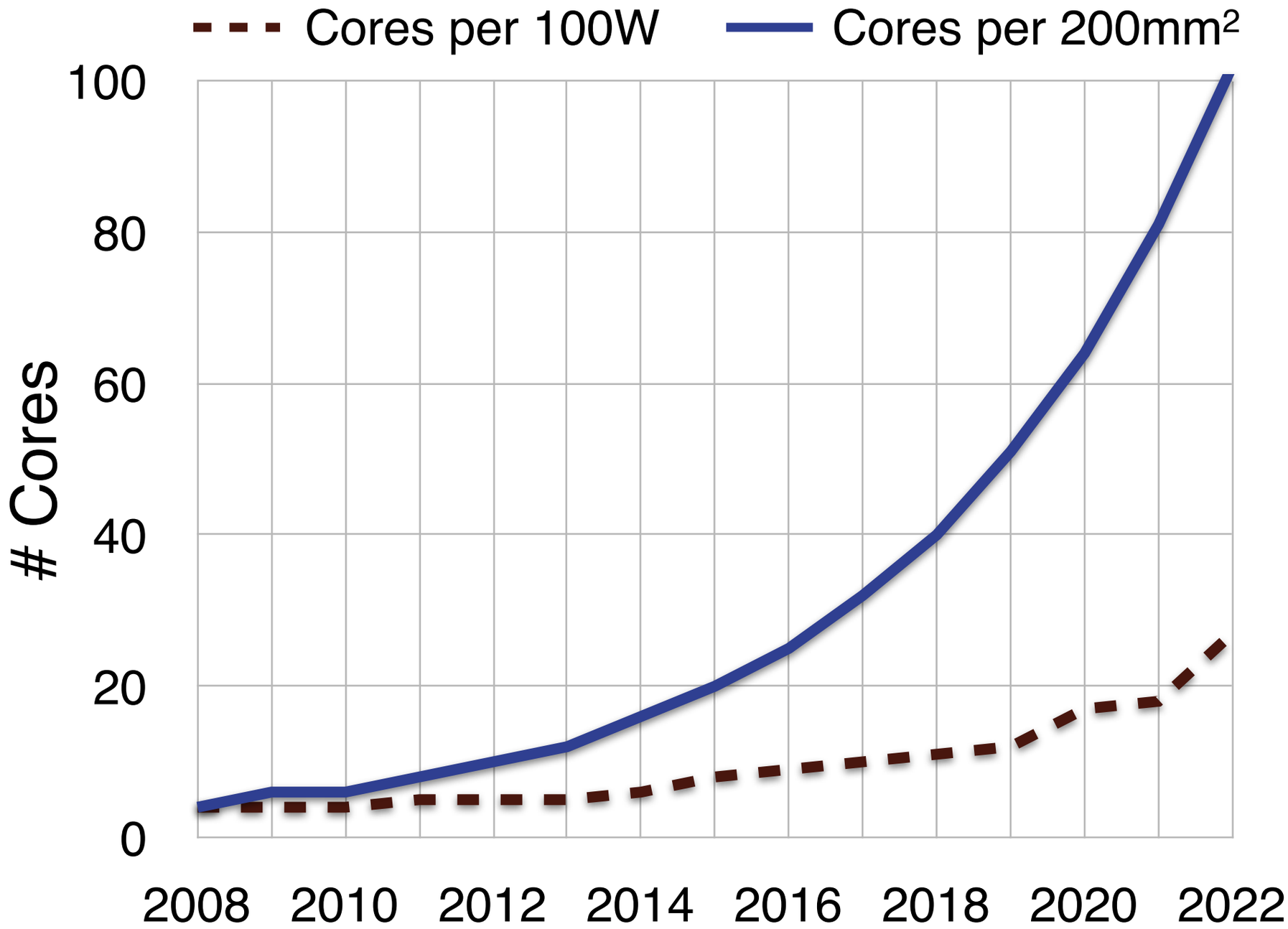

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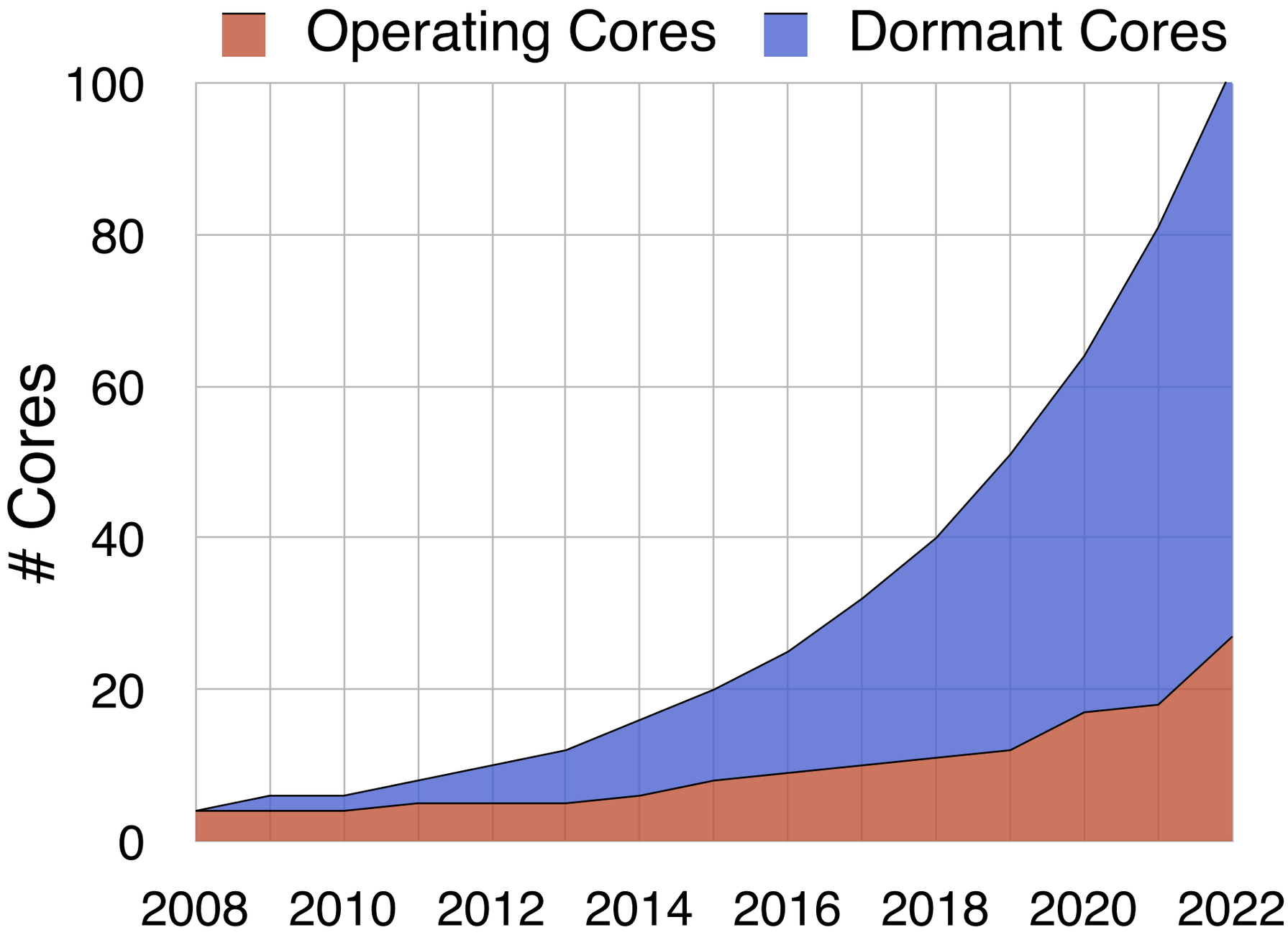

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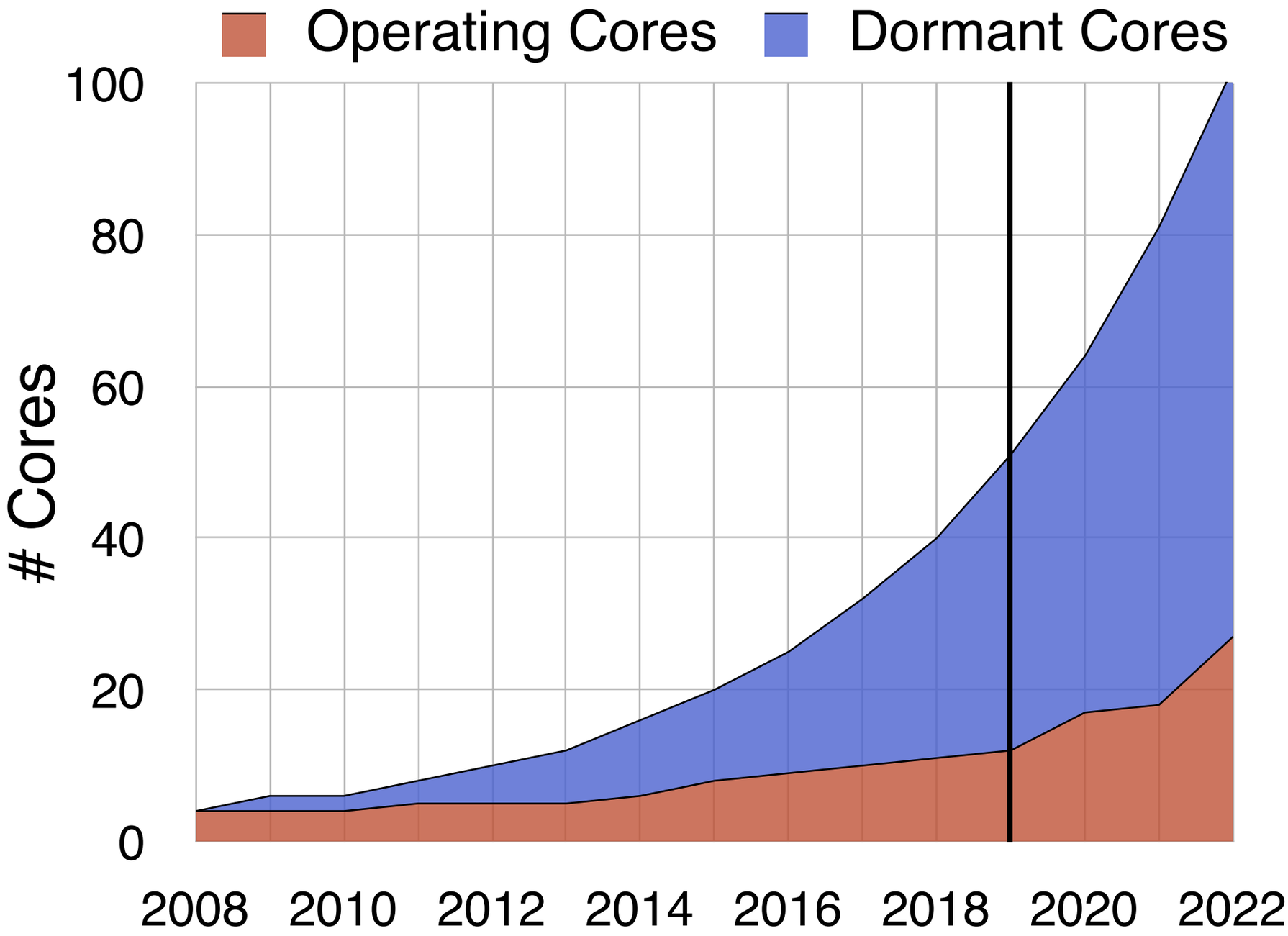
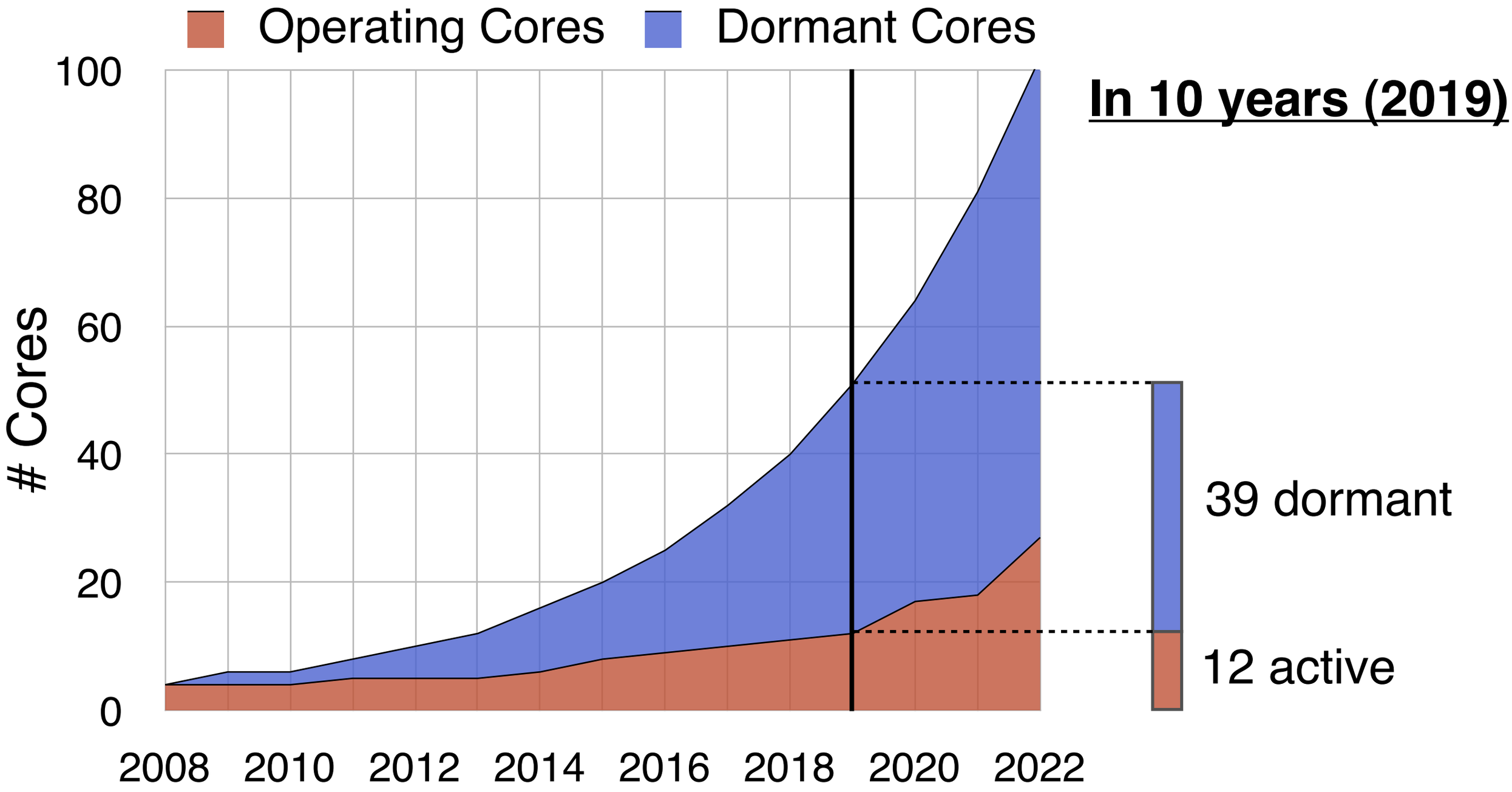


In 10 years (2019)

ITRS Power Scaling



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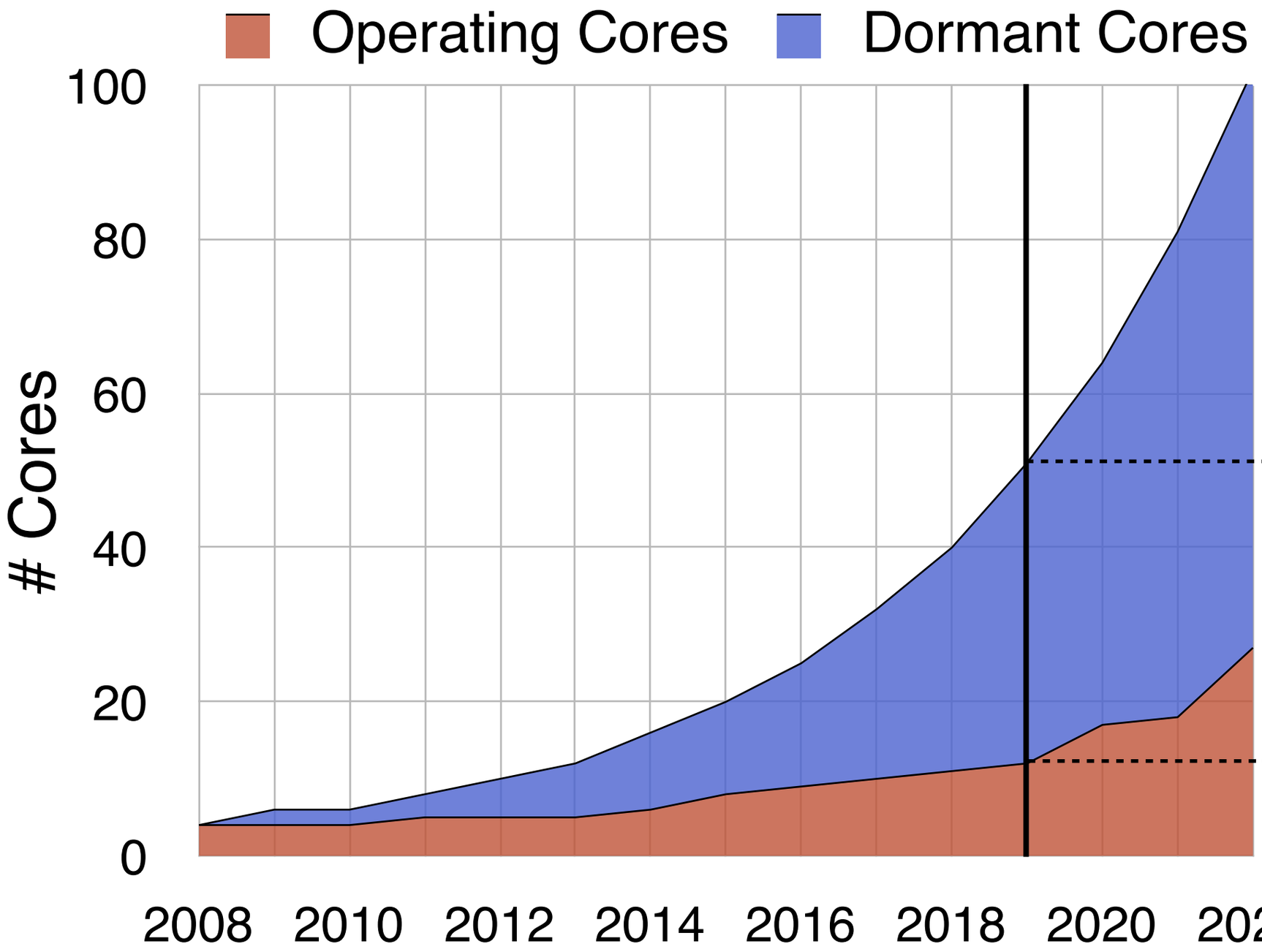

In 10 years (2019)

Only 1/4 of cores active at any time

39 dormant

12 active

Exploiting Dormant Cores

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- Chips are designed to last ~7 years

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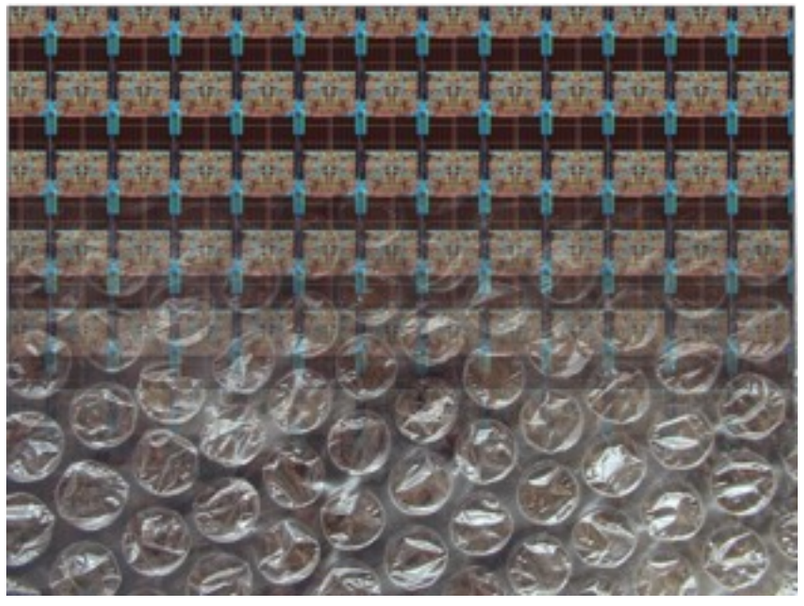
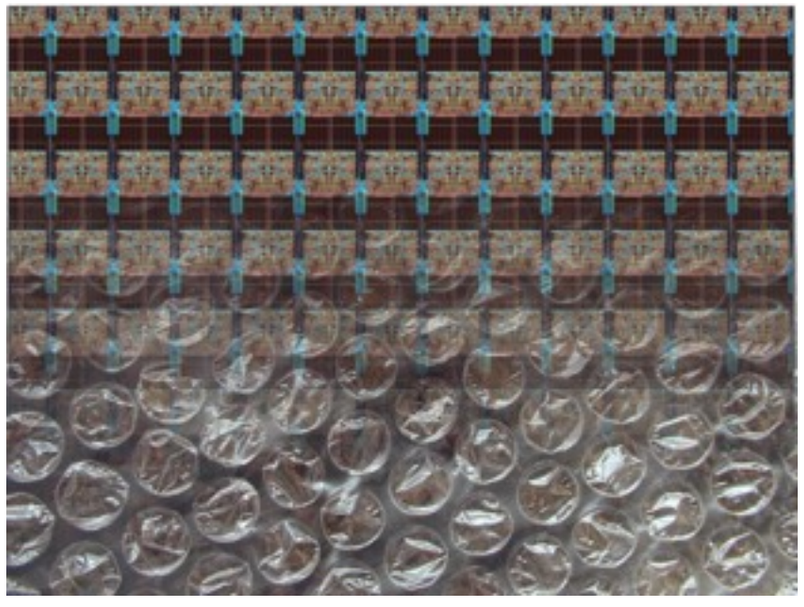


Exploiting Dormant Cores

- Chips are designed to last ~7 years

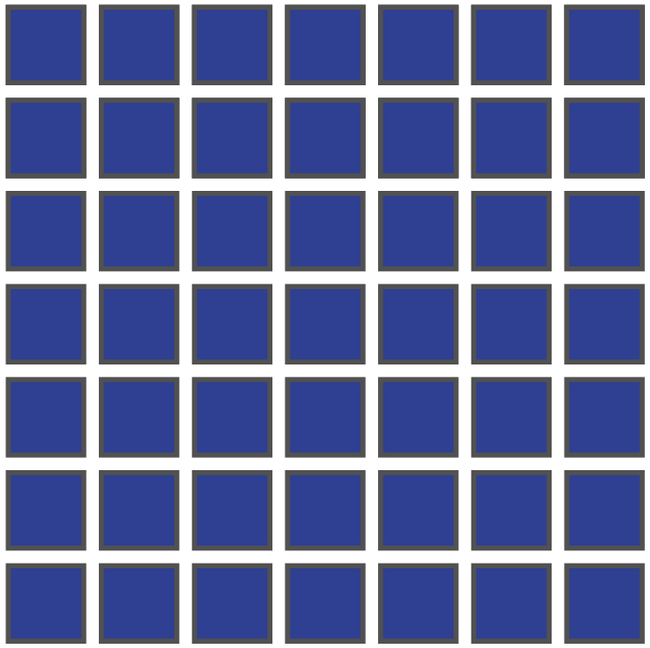
  ➡ Must operate at conservative *V*, *f*

- But we will have plenty of spare cores
  - Pop them like BubbleWrap
  - Some run at high *V*, *f* for just a few months



A BubbleWrap CMP

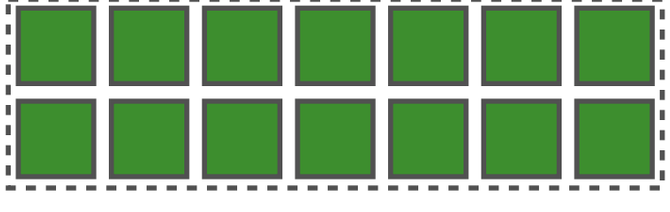
- Start with simple, homogeneous CMP

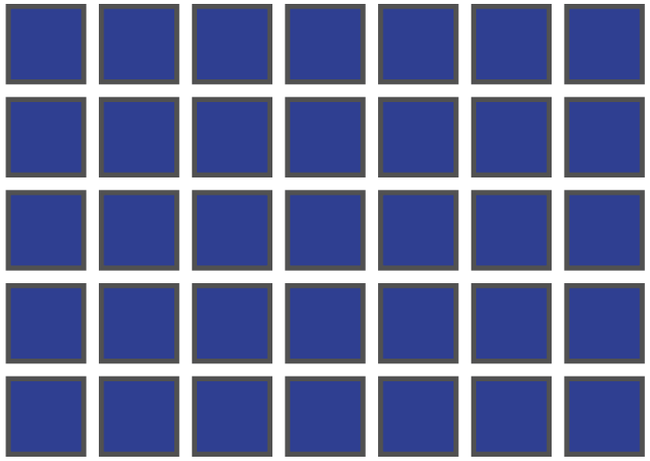


12nm CMP

A BubbleWrap CMP

Efficient, *Select* Cores

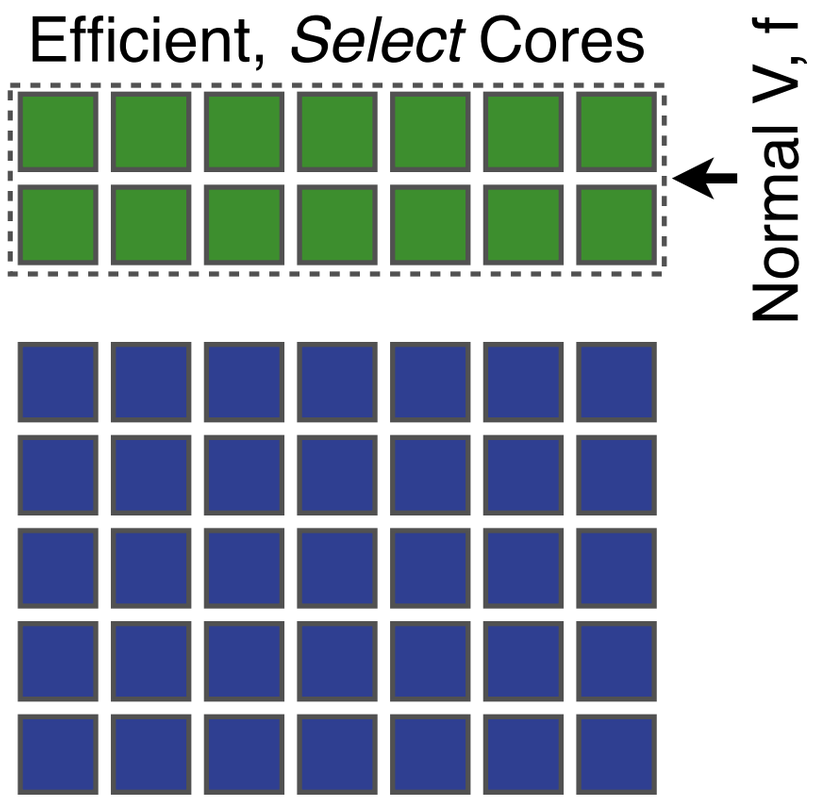




12nm CMP

- Start with simple, homogeneous CMP
- Select most efficient cores

A BubbleWrap CMP



- Start with simple, homogeneous CMP
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  - Run at nominal *V*, *f*

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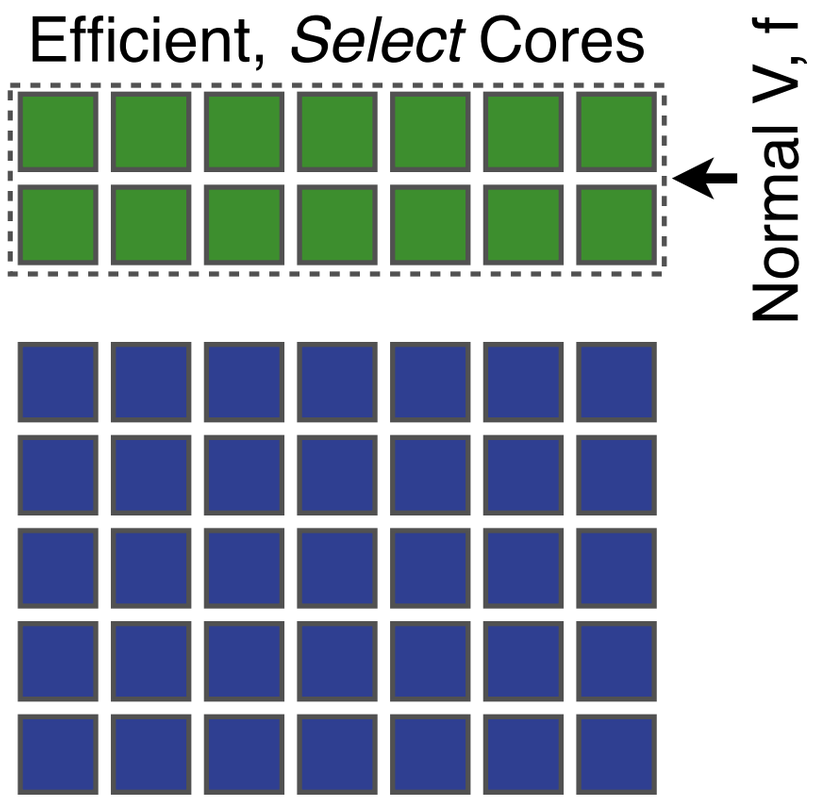

- Start with simple, homogeneous CMP
- Select most efficient cores
  - Run at nominal *V*, *f*
- Use for parallel phases

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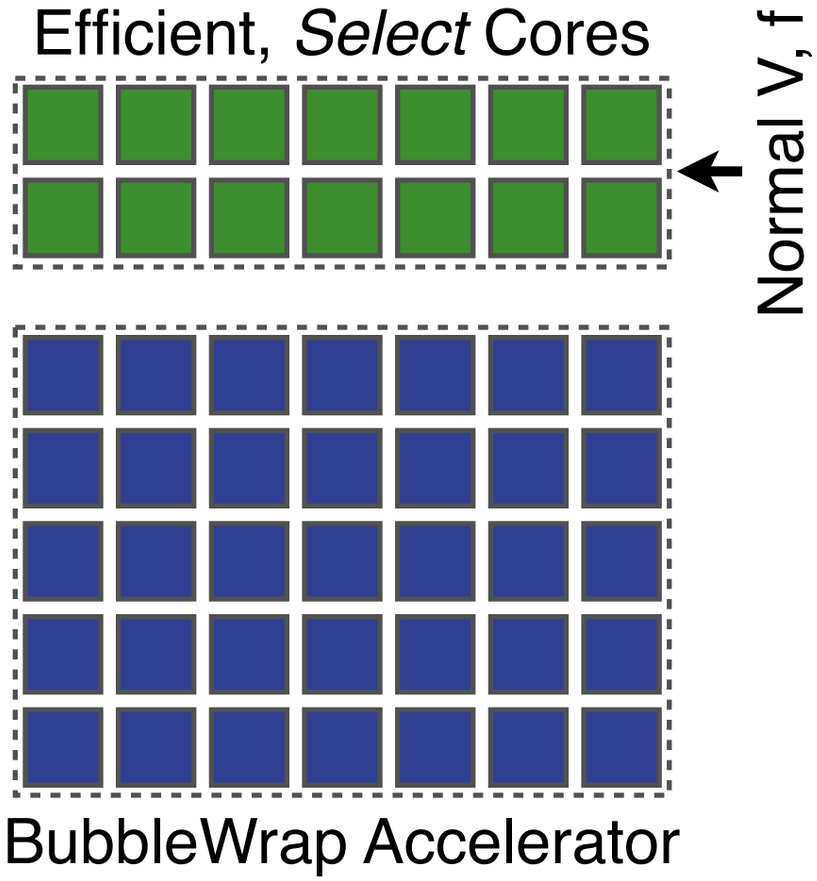

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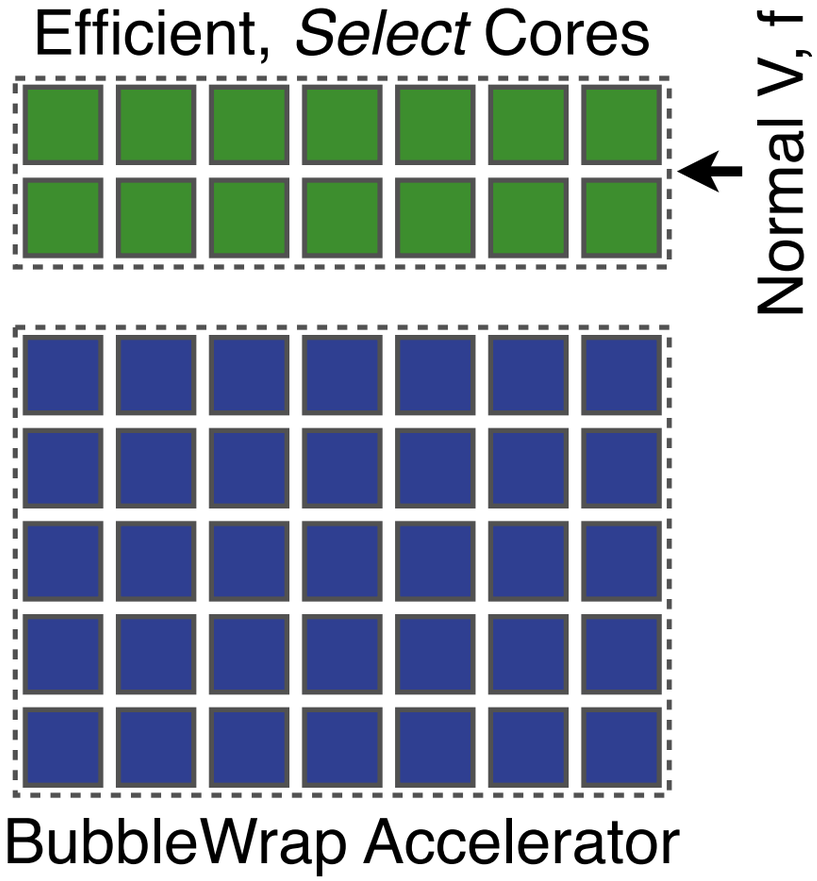

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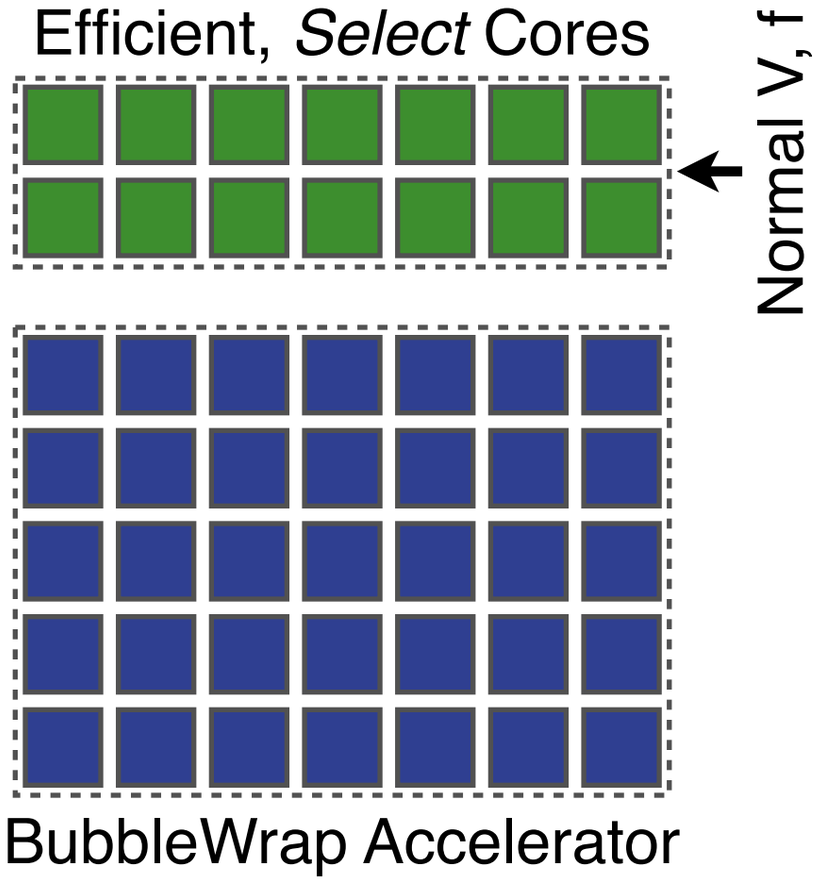

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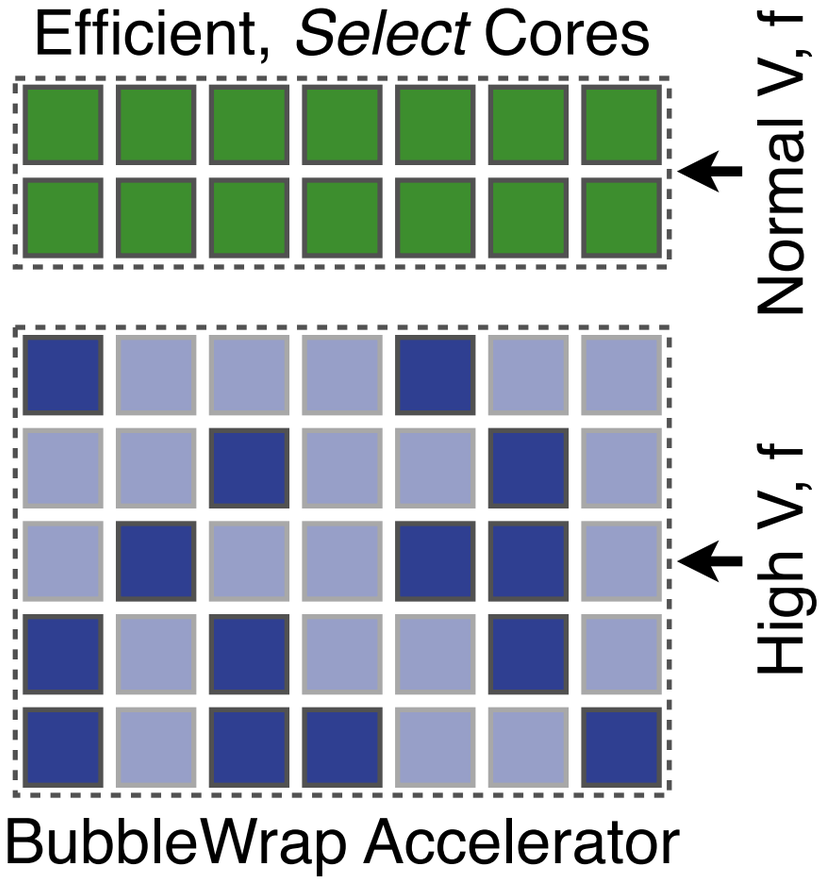

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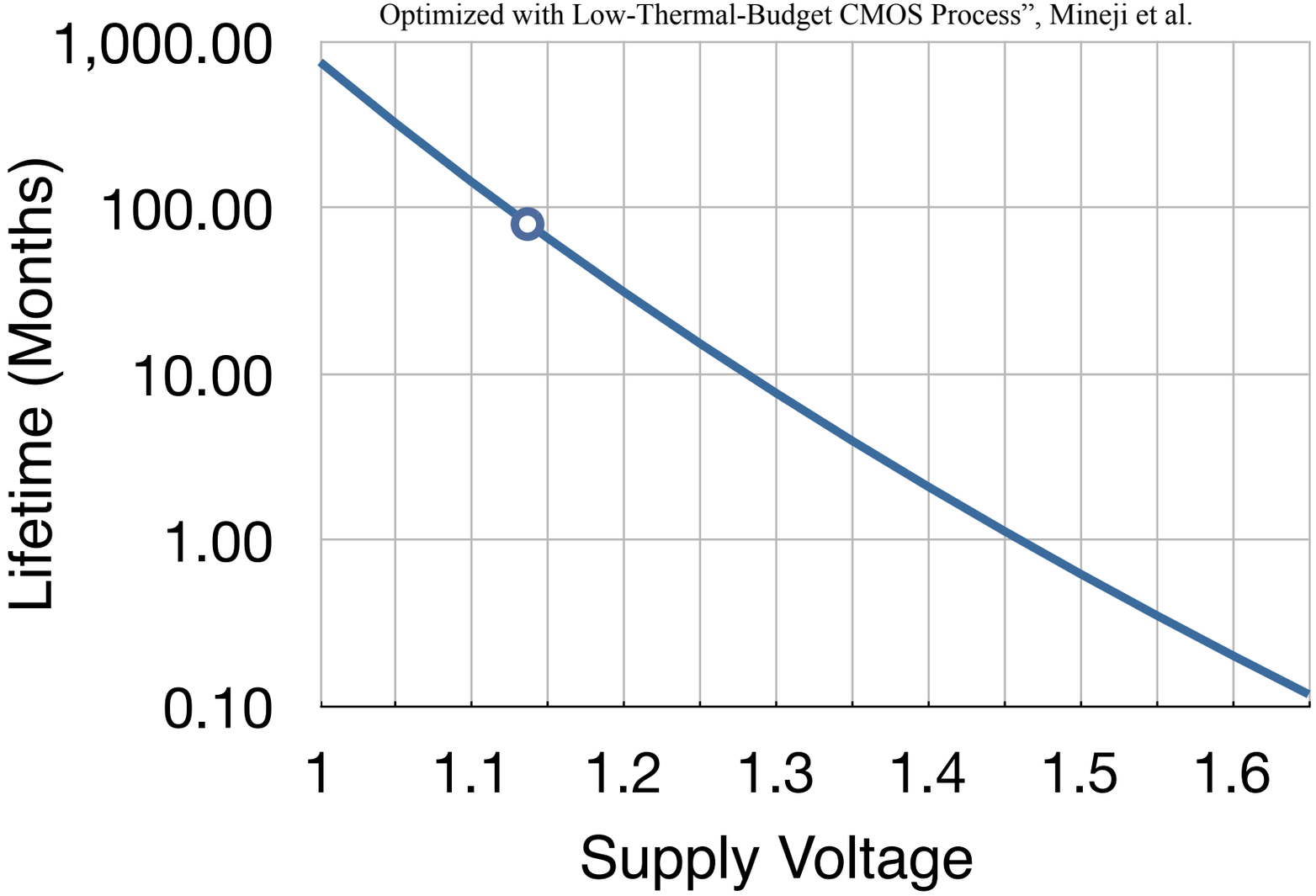
- Rest of cores are BubbleWrap
  - "Sequential accelerators"
  - Free to consume high power
  - Run at high *V*, *f*

Sequential Benefits

"Integration of Manufacturable 65nm-node HfSiON Transistors Optimized with Low-Thermal-Budget CMOS Process", Mineji et al.



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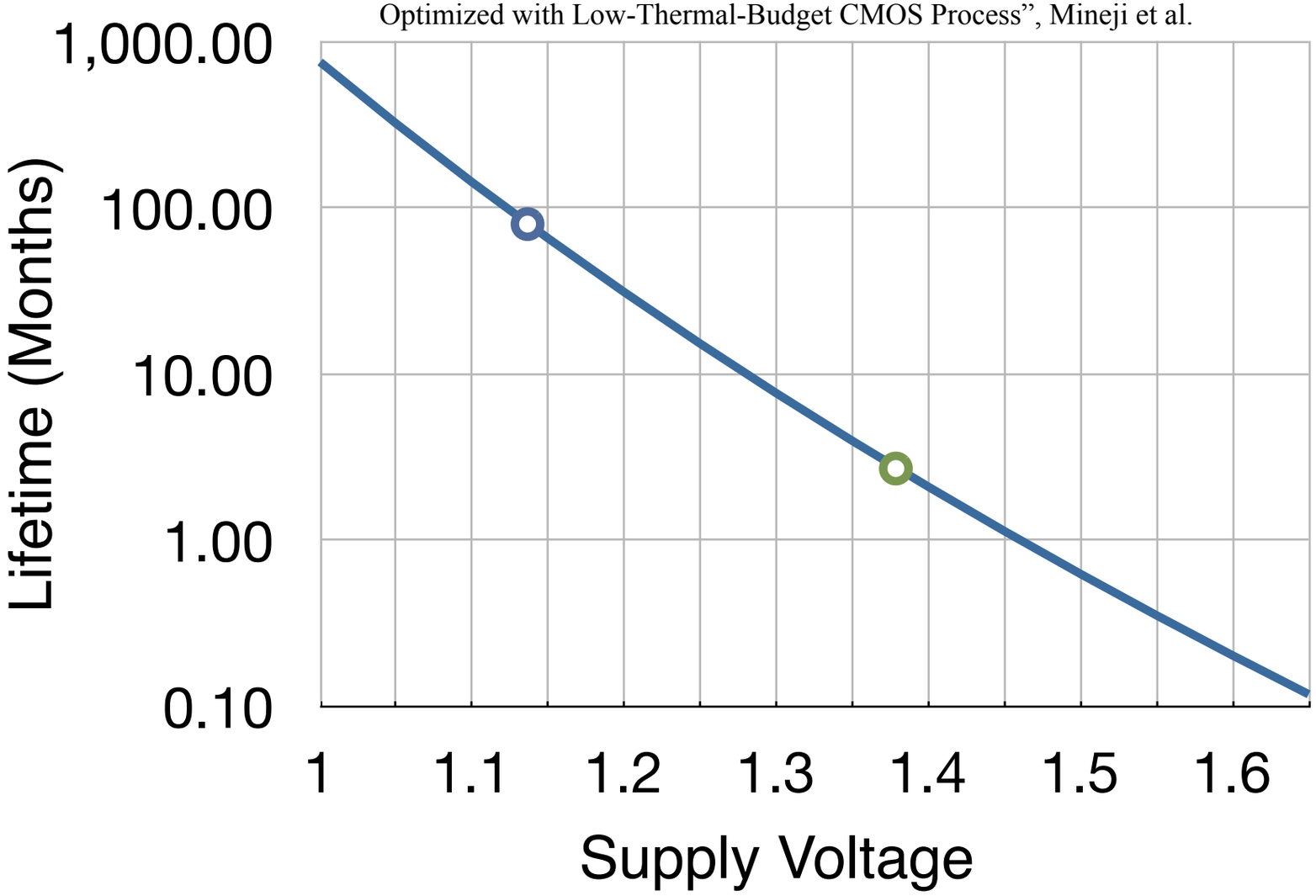

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- 35 BubbleWrap cores (2.4 months / core)

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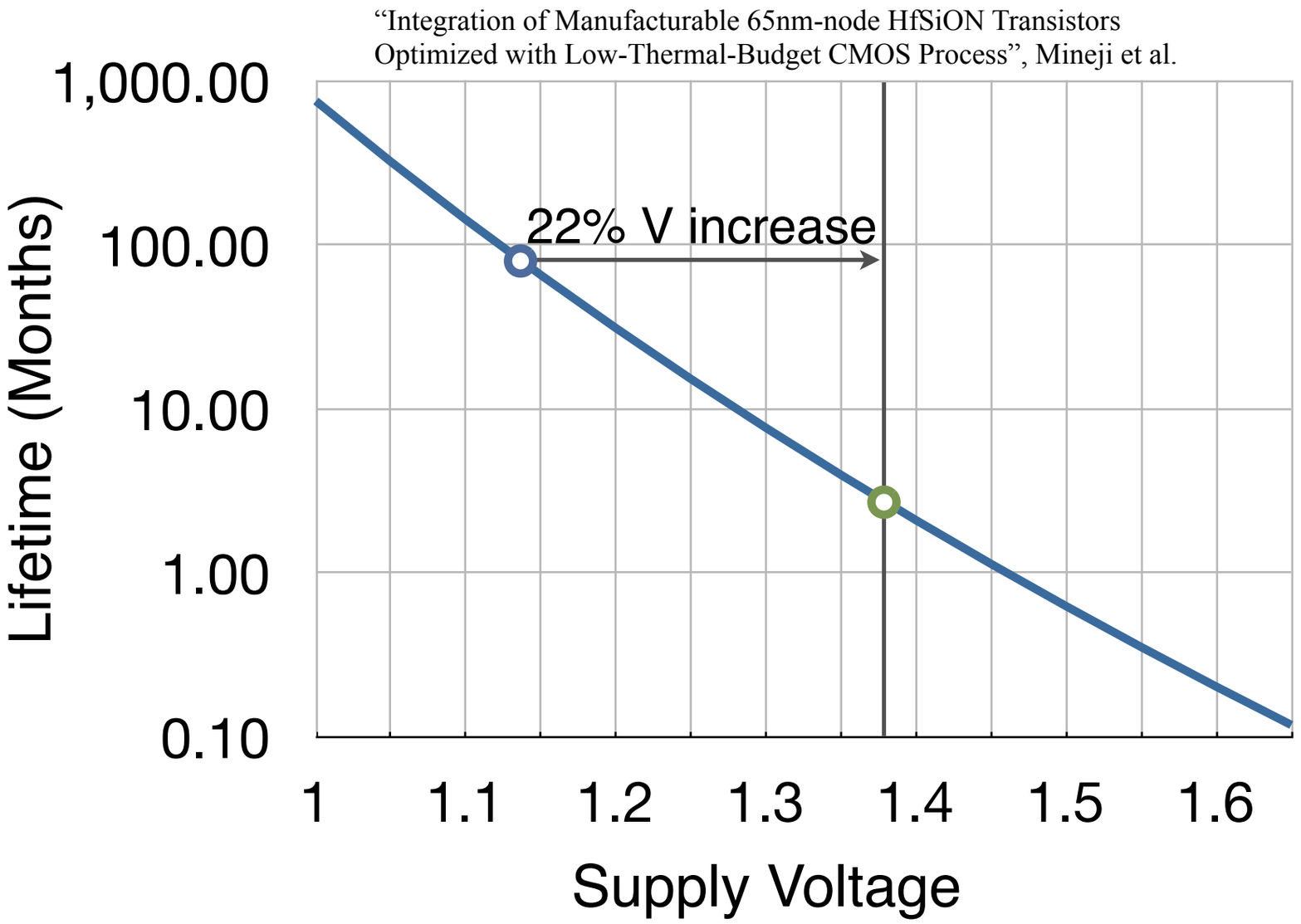

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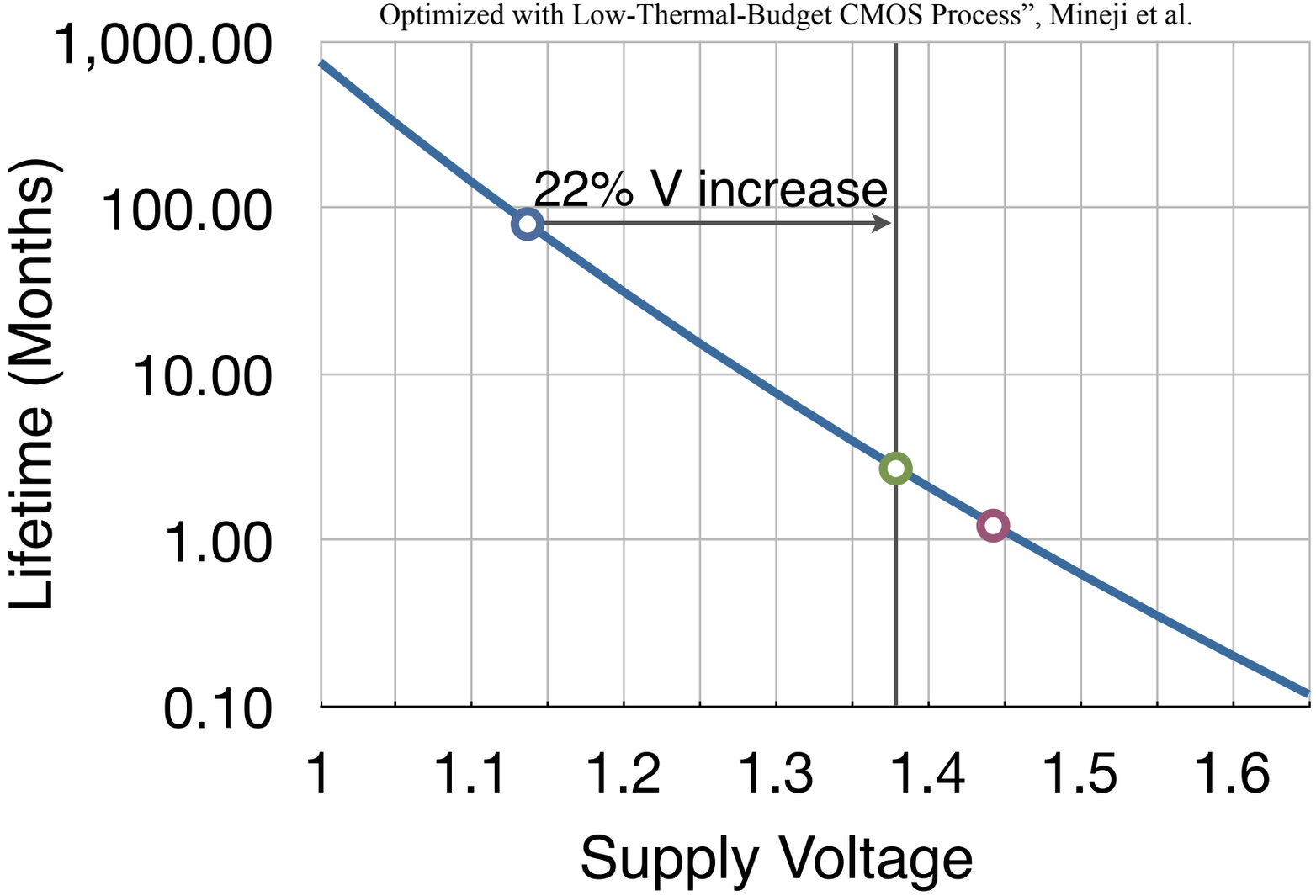

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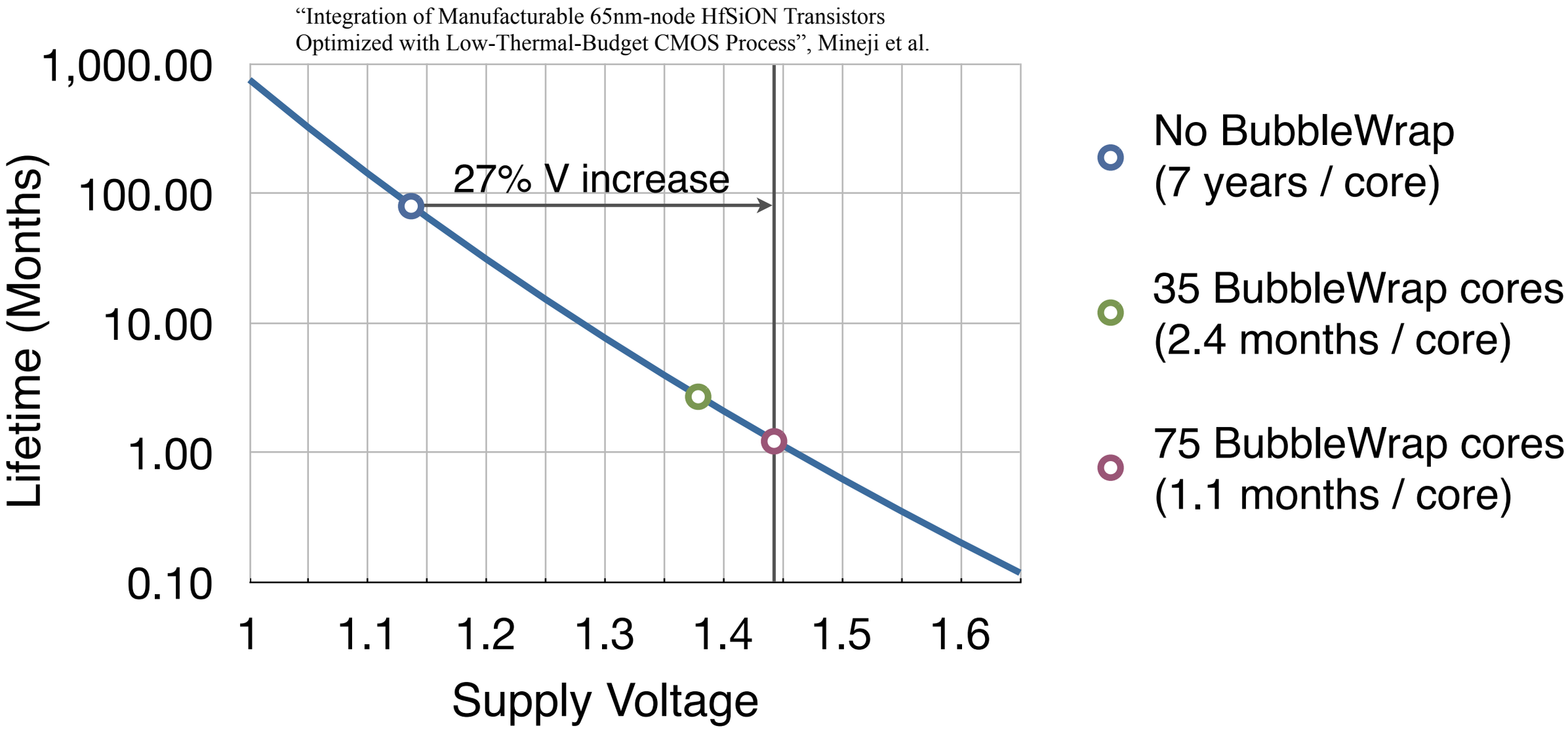
- 75 BubbleWrap cores (1.1 months / core)

Sequential Benefits



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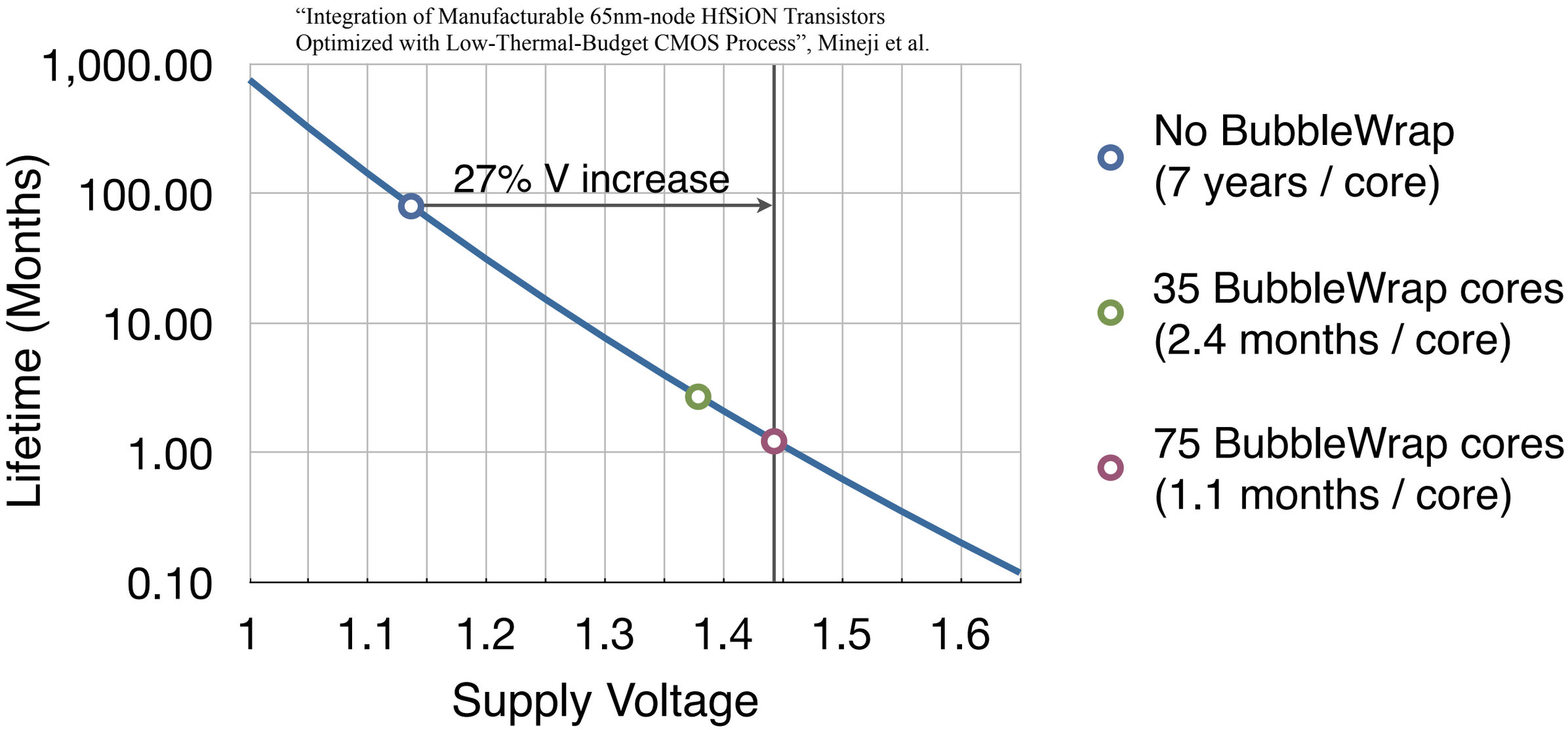


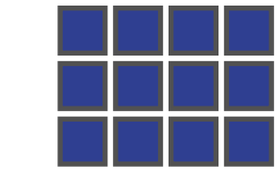
Significant single-thread frequency increase

Throughput Benefits

Throughput Benefits

- Exploit core-to-core variation in power consumption

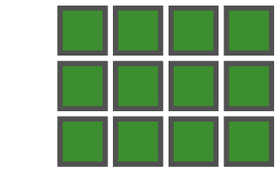
Throughput Benefits



Base CMP

- Exploit core-to-core variation in power consumption
- Base CMP: Only build as many cores as we can power

Throughput Benefits



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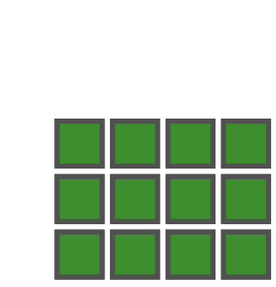

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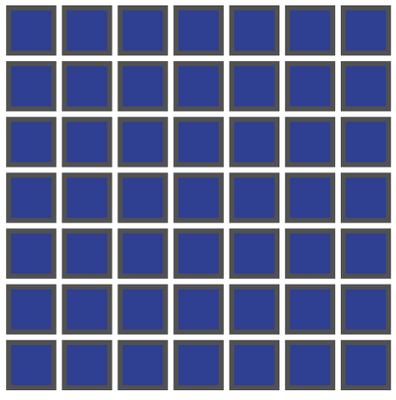

BubbleWrap CMP

- Exploit core-to-core variation in power consumption
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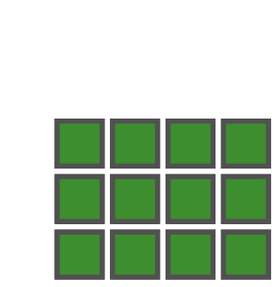
- BubbleWrap: Many cores to choose from

Throughput Benefits



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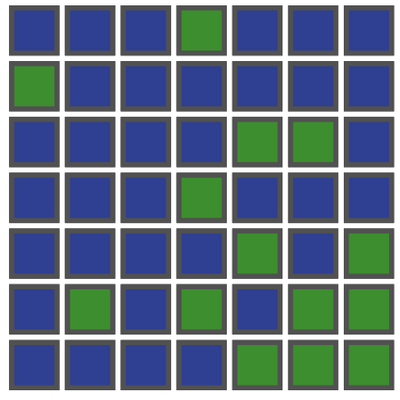

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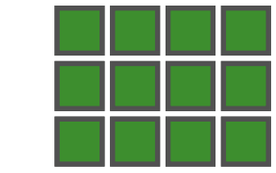

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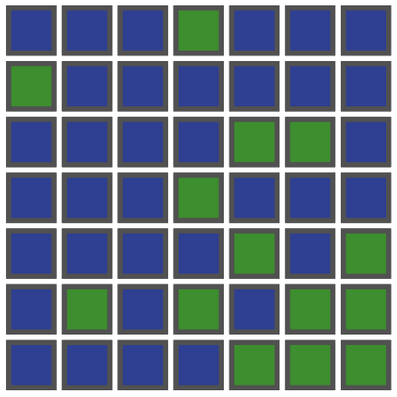

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- Base CMP: Only build as many cores as we can power
- BubbleWrap: Many cores to choose from
  - Select the most efficient ones for parallel phases

➡ 10% higher throughput than base [Teodorescu08]

Is it a good idea?

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No

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- Additional die area for dormant cores

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- Additional die area for dormant cores
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- Improves sequential *and* parallel performance
- No architectural or software changes
- Accelerates existing binaries

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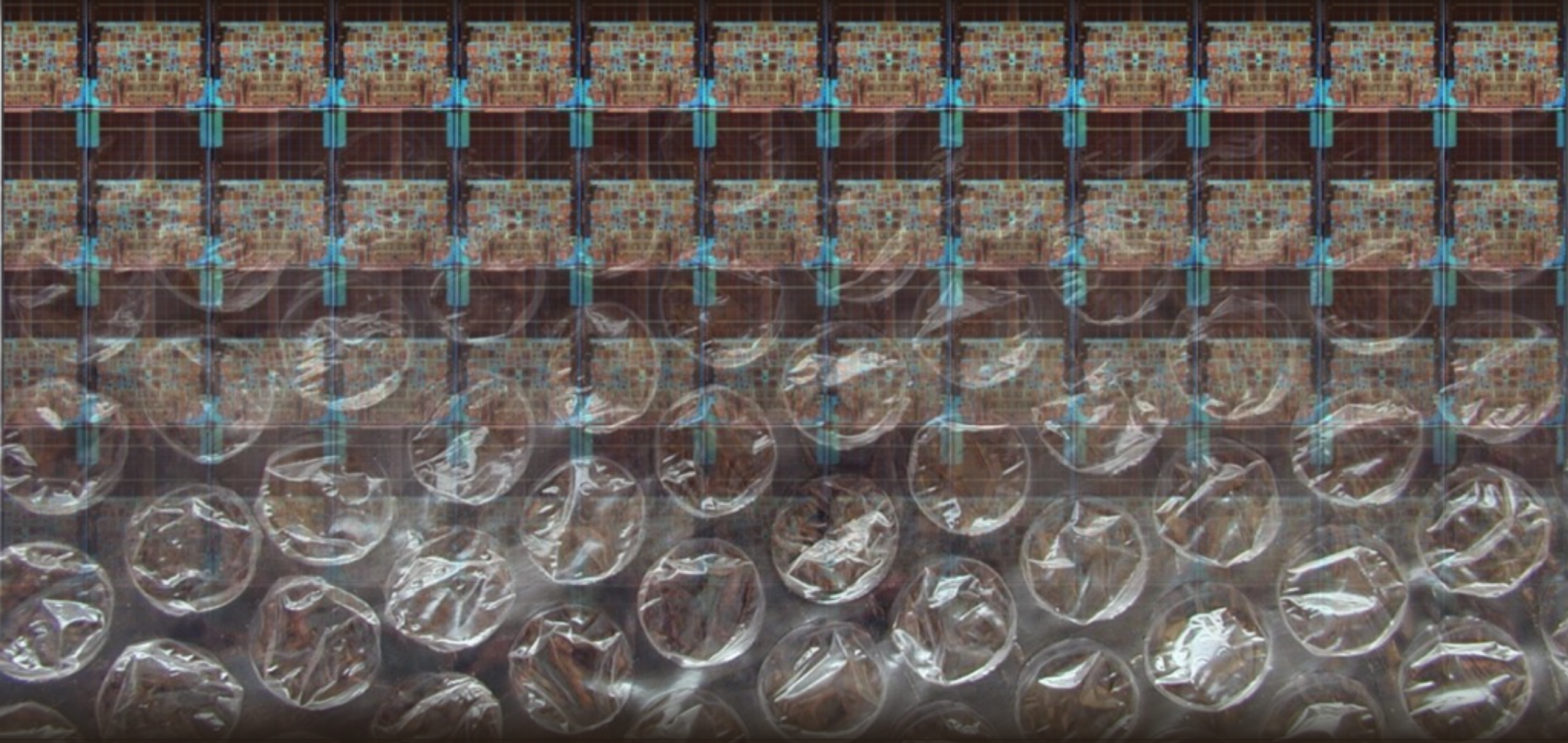

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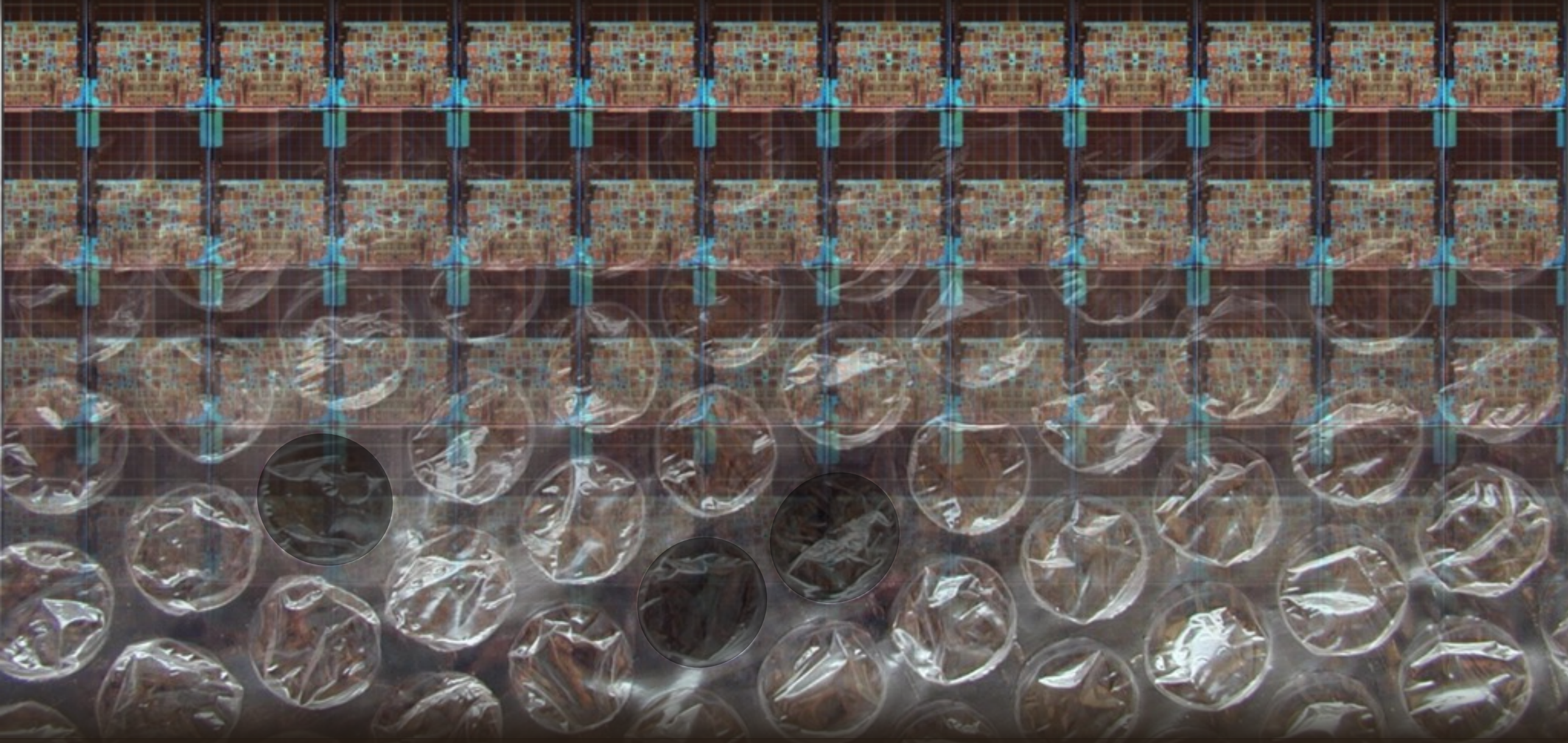

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