Outline

- Conclusion
- On-chip downloder, debugger & emulator tools
- EEPROM cell
- 12b DACs
  - 12b A-to-D converter
  - Chip block diagram / photo
- 12b Analog + EEPROM Integration Challenges
- Overview of IEEE 1451 Transducer Interface Std
KEY CONCEPT

Networks can be easily interchanged. Transducers can be specific to a network.

Field Network A

Network B

IEEE 1451.2 Transducer Interface Std
This chip:

Traditionally v. difficult to integrate due to different process complexities

Analog + EPROM Integration Challenges
True 12-bit Analog Conversion + 8b uc + Flash EEPROM

Chip Block Diagram
8-ch 12b ADC - SAR DAC Schematic
e.g. transducer offset +/- 3% can be nulled

- In-situ per-channel values,
- Factory default values, or
- Calibration coefficients:
  - Unit Cap = 14 x 13 μm (7.64fF)
- Process complexity:
  - Use Metal-Poly capacitors with calibration to simplify
  - $I_{ca} = 1.5mA_{max}$
- SAR type, 8-channel, 12b, 5µs conversion

12b Analog-to-Digital Converter
Internal EEPROM from Code executing

THD = -77.4dB
SNR = 69.5dB

ADC test mode
uc halted

Temp = 25°C
FS = 25kHz
Fin = 2kHz
Vref = +5V
VCC = +5V

ADC SNR + THD
External memory

In DMA mode, ADC converts at max 5+5 rate and stores result directly in external memory, e.g., for FFT analysis.

- ADC takes ~ 1IS per instruction @ Fclk 12MHz...

ADC DMA Mode
12b Digital-to-Analog Converter

V_{out} \approx 1540

unit R = 30 \times 1.3 \text{pm poly}
DNL > 1 LSB

Ieqa > 400μA

Tconv = 10μs min (RL > 10kΩ, CL > 200pF)

Two 0.33 LSB typ DNL

Two on-chip PWM

Two Cypress Microchip; no need to use timers for PWM output

Resistor string multiplying architecture; buffered output

12b Digital-to-Analog Converter
Split-Gate Flash EEPROM Cell
User's target board

Support

Emulation

debug &

Industry std

Chip has

10.5KB EEPROM

Data

Port 0

Addr

Control

Port 2

Port 3

Vpp

NC

CHIP SUPPORTS INDUSTRY STANDARD 3RD PARTY TOOLS

SOFTWARE SUPPORT - I

DEBUG & EMULATION:

Gang Programmer:

PARALLEL PROGRAMMING:

© IEEE 1998
User's target board

preserved
analog performance
... debugger & emulator
Chip has on-chip

On-chip in-situ debugging/emulation:
... no clips or pods:

User's target board

UART & Charge Pump
using on-chip
Download & Program

On-chip Downloader:

- Chip has downloader, debugger, emulator on-chip:

Software Support II - extra on-chip tools
2 rows (64 bytes)
MIN ERASE SECTOR

MEMORY ARRAY
8K CODE

2K BOOTSTRAP

EMULATOR
DEBUGGER
DOWNLOADER
PWRL-UP LOADER

EEPROM BLOCK
Power Dissipation

Sensor Input

Smart Transmitter ADC

Power Loop

VCC = 3V

VCC = 5V

25°C

1st silicon, Dac Off.

12MHZ

Flick

20MA

10MA

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Conclusions