18-345
Introduction to Telecommunication Networks
Homework 2 Solution

September 23rd, 2007 **Due: September 29th, 2007**

1. ATM uses an eight-bit CRC on the information contained in the header. The header has six fields:

First 4 bits: GFC field
Next 8 bits: VPI field
Next 16 bits: VCI field
Next 3 bits: Type field
Next 1 bit: CLP field
Next 8 bits: CRC

The CRC is calculated using the following generator polynomial g(x):
$x^8 + x^2 + x + 1$.
Find the CRC bits if the GFC, VPI, Type, and CLP fields are all zero, and the VCI field is 00000000 00001111. Assume the GFC bits correspond to the highest-order bits in the polynomial.

Solution:
$g(x) = x^8 + x^2 + x + 1 = 100000111$
GFC = 0000, VPI = 0000 0000, VCI = 0000 0000 0000 1111,
Type = 000, CLP = 0, CRC bits = 0000 0000
Therefore the polynomial can be written as:
0000 0000 0000 0000 0000 0000 1111 0000 0000 0000
$= x^{15} + x^{14} + x^{13} + x^{12}$

```
                      1111 0010
100000111  | 1111 0000 0000 0000
           | 1000 0011 1
             ---------------------
              111 0011 10
              100 0001 11
             ---------------------
               11 0010 010
               10 0000 111
             ---------------------
                1 0010 1010
                1 0000 0111
             ---------------------
                    10 1101 000
                    10 0000 111
             ---------------------
                      1101 1110
```

CRC = 11011110

2. A proposed encoding scheme applies 6 error correction/error detection bits to a 16-bit long data word. The probability of a bit being in error is PB, and is an independent random variable. This encoding scheme promises that all single bit errors can be corrected, and all double will be detected (but not corrected). Assuming that all combinations of three or more errors will not be detected or corrected, find mathematical expressions for:

a) The probability that no errors occur
b) The probability that a correctable error occurs
c) The probability that a detectable but not correctable error occurs
d) The probability that an undetectable/uncorrectable error occurs

Solution:

a) The probability that no errors occur

$$P_1 = (1 - PB)^{22}$$

[Note: 22 because that is the total length of the codeword is 16 + 6 = 22]

b) The probability that a correctable error occurs

$$P_2 = \binom{22}{1} PB\,(1 - PB)^{21}$$

c) The probability that a detectable but not correctable error occurs

$$P_3 = \binom{22}{2} PB^2\,(1 - PB)^{20}$$

d) The probability that an undetectable/uncorrectable error occurs

$$P_4 = 1 - (P_1 + P_2 + P_3)$$

3. Given a set of codewords, the "minimum Hamming distance" is defined as the smallest number of bits that two codewords differ. For example, the minimum Hamming distance of the set of codewords{000 , 001 , 111} is 1.

a) Determine the minimum Hamming distance of the following set of codewords.

1100110111001
1000101001001
1101000110100
0111011110101

b) One of the codewords from the set given above is transmitted across a noisy channel, and d is received as: 1100000110000. Given that the received sequence has 2 bit-errors, is it possible to detect the errors? Correct the errors?

Solution:

a) Since any two codewords of the set differ in at least 5 bits, while the 1st and 2nd codewords differ in exactly 5 bits, the minimum Hamming distance for this set of codewords is 5.

b) Correcting the received codeword is simply a matter of finding the allowed codeword that is closest (smallest Hamming distance) to the received codeword. In this case, the answer is 1101000110100. The reason that we can correct this properly is that with 2 bit errors, the received vector lies within the sphere of the transmitted codeword, because the minimum Hamming distance is 5.

With a hamming code with distance d, we can detect t <= d - 1 errors i.e. 4 errors and correct t <= (d-1)/2 = 2 errors.

4. Suppose a multiplexer in a TDM (circuit switched) network has two input streams, each at a nominal rate of 1 Mbps. To accommodate deviations from the nominal rate, the multiplexer transmits at a rate of 2.2 Mbps as follows. Each group of 22 bits in the output of the multiplexer contains 18 positions that always carry information bits, nine from each input. The remaining four positions consist of two flag bits and two data bits. Each flag bit indicates whether the corresponding data bit carries user information or a stuff bit because user information was not available at the input.

a) Suppose that the two input lines operate at exactly 1 Mbps. How frequently are the stuff bits used?

b) How much does this multiplexer allow the input lines to deviate from their nominal rate?

Solution:

a) The frame rate of the output line is 2.2/22 = 100 kHz. In this case, the stuff bits are always used because the information bits alone provide an aggregate bit rate of (100 kHz)*18 = 1.8 Mbps. With the two extra data bits, the aggregate bit rate is (100 kHz)*20 = 2 Mbps.

b) This multiplexer provides either 9 or 10 bits for each stream per 22-bit frame.

Thus, it allows either of the two input streams to transmit as low as (100 kHz)*9 =

0.9 Mbps and as high as (100 kHz)*10 = 1.0 Mbps.

5. SONET allows positive or negative byte stuffing to take place at most once every four frames. Calculate the minimum and maximum rates of the payload that can be carried within an STS-1 SPE.

Solution:

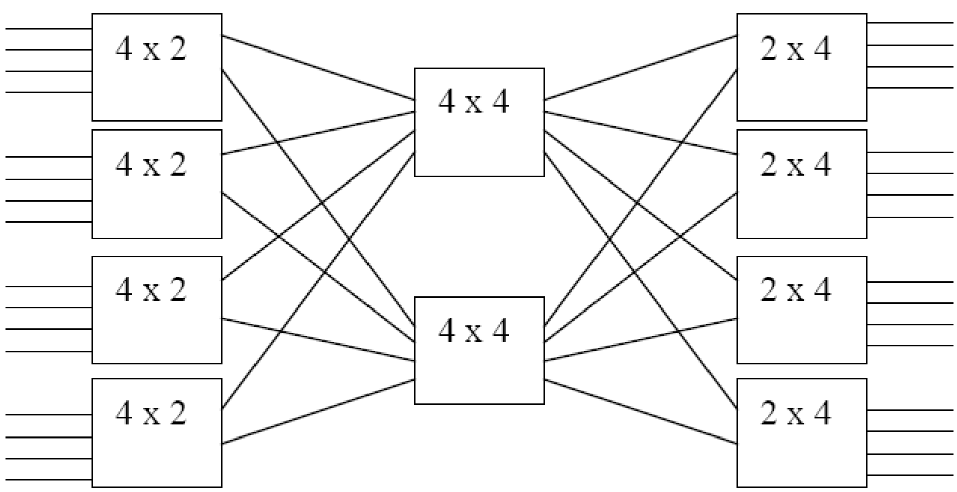
STS-1 rate = 51.84 Mbps
Nominal Payload rate = 9*87*8000 = 6.264 Mbytes/s = 50.112 Mbps
Frame = 125 μsec
Drifts = (8 bits) / (4 x 125 μsec) = 0.016 Mbps
Maximum payload rate = 50.112 + 0.016 = 50.128 Mbps
Minimum payload rate = 50.112 – 0.016 = 50.096 Mbps

6. Consider the multistage switch in Figure 4.35 in the textbook with N = 16, n = 4, k = 2.

a) What is the maximum number of connections that can be supported at any given time? Repeat for k = 4 and k = 10.
b) For a given set of input-output pairs, is there more than one way to arrange the connections over the multistage switch?

Solution:

a) For N = 16, n = 4 and k = 2, we have the following switch architecture:



Thus, the second stage is the bottleneck, and blocking can occur in the first stage.
Thus, eight connections can be supported at a time.

If k = 4, 16 connections can be supported at a time. However, blocking will occur if we are not allowed to rearrange connections. It can be shown that in this case blocking can be avoided if we are allowed to rearrange the connection pattern every time a new connection request is made.

If k = 10 ≥ 2n-1 = 7, then there are ten 4 x 4 switches in the second stage and the switch is non-blocking. The switch can accommodate any set of connections without blocking.

b) As shown in the picture in part (a), it is clear that each input-output pair can be connected through any one of the k second-stage switches. Thus, there are k ways to arrange the connections over a multi-stage switch.

7. Illustrate graphically the complexity of a crossbar switch and the complexity of a Clos network relatively to N (= #inputs = #outputs). Briefly describe what you observed from the graph.

Solution:

Complexity of crossbar switch: N^2

For Clos Network: #crosspoints = $2(N/n)nk + k\,(N/n)^2$ **(non-blocking: $k \geq 2n-1$)**

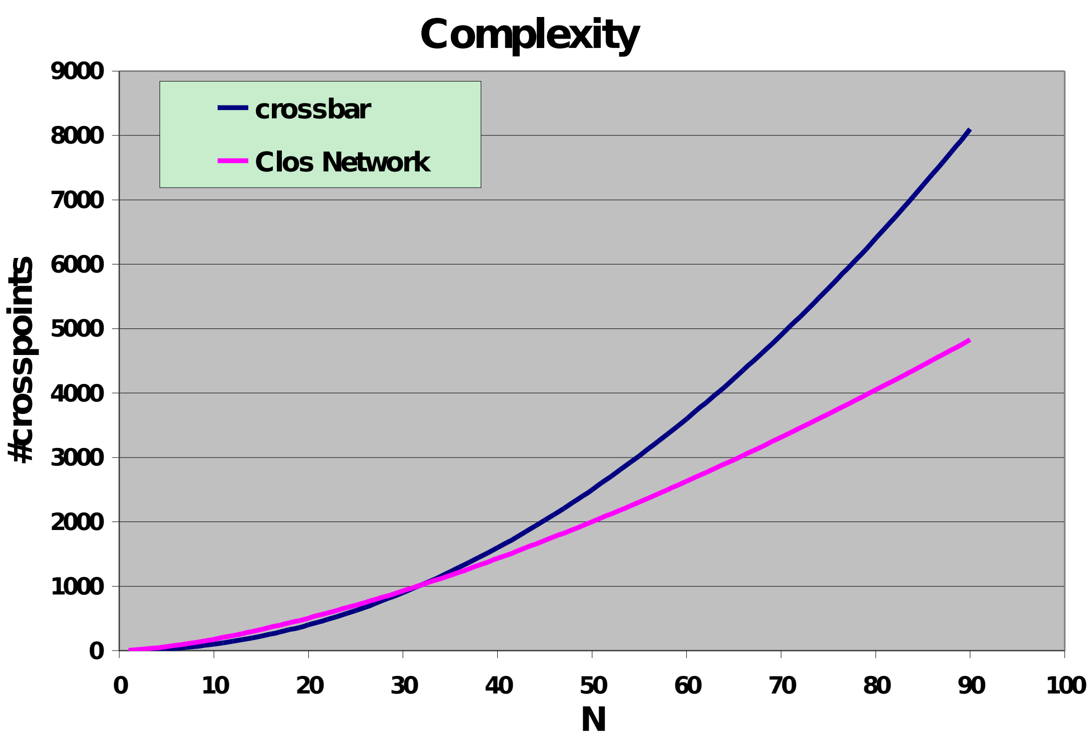
We pick $k = 2n - 1$ such that the total number of crosspoints is minimized.

#crosspoints = $\mathbf{2N(2n-1) + (2n-1)\,(N/n)^2}$

By differentiating the above expression with respect to n, we get $\mathbf{n \approx (N/2)^{1/2}}$.

Therefore, the complexity of Clos network:

$$2N\,(2(N/2)^{1/2}-1) + (2(N/2)^{1/2}-1)\,(N/(\,(N/2)^{1/2})\,)^2 \approx 4\sqrt{2}\,N^{3/2}$$



As N increases, the complexity of crossbar increases much faster than that of Clos Network.