

# Hybrid Hall Effect Devices – A Novel Building Block For Reconfigurable Logic

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The volatile nature of the SRAM cells that hold configuration state in most current reconfigurable logic devices is a significant limitation, requiring that the device be re-programmed each time power is applied. In this paper, we present a new class of reconfigurable logic elements based on magnetoelectronic devices, known as hybrid Hall effect (HHE) devices. HHE devices can be configured on a cycle-by-cycle basis to compute a variety of logic functions, and retain their state indefinitely even in the absence of an external power supply. In this paper, we present a number of reconfigurable circuits that illustrate the capabilities of the HHE device and show how it can be integrated with conventional CMOS systems.

## 1 Introduction

Silicon CMOS is the most commonly-used implementation technology for reconfigurable logic devices today because of the high device densities that it offers. However, CMOS-based reconfigurable logic systems have the disadvantage that they are volatile, requiring the

presence of a power supply to retain their configuration and other state. In many systems, this means that an additional non-volatile memory is required to hold the configuration state of any reconfigurable logic when the system is powered down, increasing the cost of the system. In addition, the time required to configure the reconfigurable logic at power-on is a significant drawback for systems that require instant-on operation.

In this paper, we present a set of reconfigurable logic circuits based around hybrid Hall effect devices, which integrate a ferromagnetic element with more-conventional semiconductor structures to deliver cycle-by-cycle reconfigurability and non-volatile operation. The paper begins with a description of the HHE device and its function. We then present several reconfigurable circuits based on this device, and conclude.

## 2 HHE Device Description and Operation

The hybrid Hall effect (HHE) device [3,5] is a semiconductor structure that contains a ferromagnetic element (FE) for non-volatile storage. Like other ferromagnetic devices [1,4,6], the HHE device relies on the stability of the magnetization of ferromagnetic materials to retain its state in the absence of a power supply, but the specifics of the HHE device make

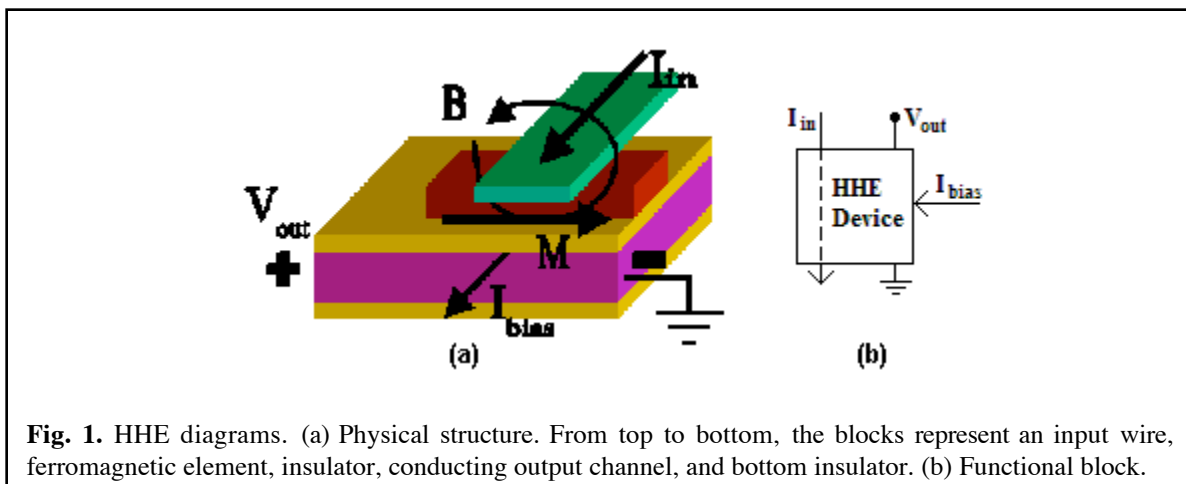
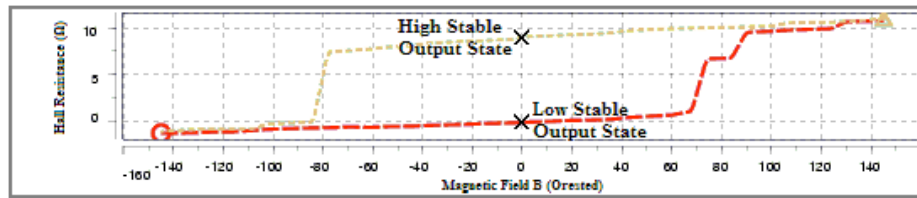


Fig. 1. HHE diagrams. (a) Physical structure. From top to bottom, the blocks represent an input wire, ferromagnetic element, insulator, conducting output channel, and bottom insulator. (b) Functional block.



**Fig. 2.** Hysteresis Loop. Top curve represents high output state. Bottom curve represents low output state. The direction of the magnetization switches  $\sim \pm 90$  Oersted, which corresponds to moving from the bottom curve to the top curve or vice versa

it uniquely suited to reconfigurable logic applications.

The physical structure of the HHE device is shown in Fig. 1 along with a functional block diagram. The functional block diagram is an abstraction of the physical structure and contains 3 main terminals – an input line, an output line, and a read bias line.

Inputs to the HHE device are currents. The directions of these currents are analogous to Boolean logic values at the HHE inputs. The purpose of these current inputs is to influence the magnetization of the ferromagnetic element. Fig. 1(a) shows that a right magnetization  $M$  is inductively coupled to the above input line with induced field  $B$ . An input current in the opposite direction will influence a left magnetization.

The ferromagnet has two stable magnetized states that are oriented to either the left or the right. For small currents  $I$ , the ferromagnet retains its present state. When the current  $I$  exceeds the switching threshold of the ferromagnetic element, the magnetization state will align with the induced field  $B$ .

According to the Hall effect, the magnetized

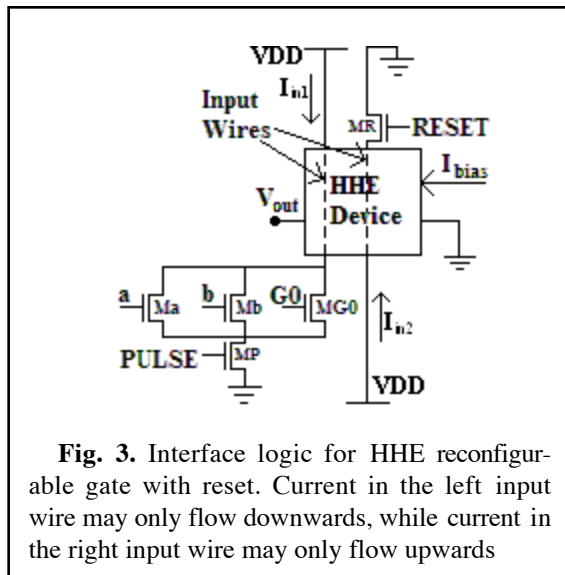
direction of the ferromagnet will create either a positive or negative output voltage. This voltage requires a read bias current to be sensed and is proportional to the read bias current by the Hall resistance. By adding a slight fabrication offset, [5] shows that the HHE outputs may be mapped to CMOS logic levels with one logic level at  $\sim 0$  Volts and the other at  $V_{DD}$ .

The behavior of the HHE device is summarized by the hysteresis graph in Fig. 2. The input magnetic field  $B$  is proportional to the input current  $I$ . When no input current exists, there are two stable output states at  $B=0$ . The two curves correspond to the current directional state of the FE magnetization.

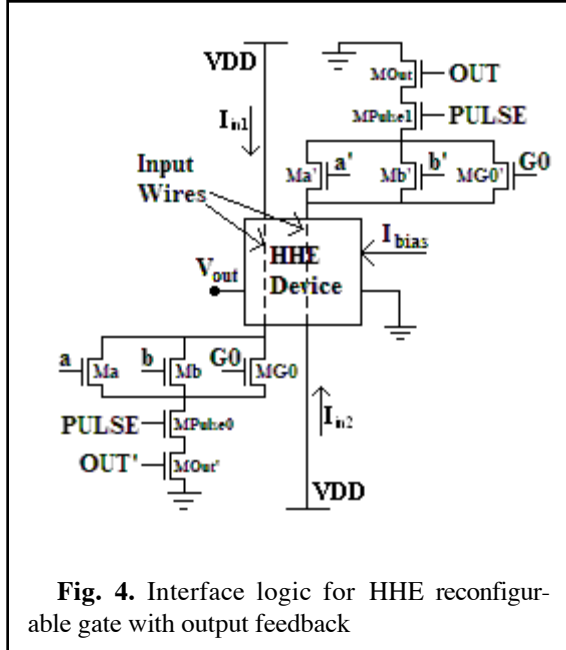
The physical dimensions of current HHE devices are approximately  $100 \mu\text{m}^2$ . However, these dimensions are expected to shrink to below  $10 \mu\text{m}^2$  in the near future. As device dimensions shrink, the HHE device characteristics will improve. Projected switching thresholds are  $\sim 10\text{mA}$  at the HHE inputs. This value is assumed for simulated devices presented later.

### 3 HHE Reconfigurable Gate with Reset

To simplify integration of HHE gates into semiconductor systems, we assume that conventional voltage-based signaling will be used to convey logic levels between HHE gates, and surround each HHE gate with interface logic that converts these voltage levels into the currents required by the gate. To simplify this logic, we assume a two-input HHE device, in which two input wires are stacked vertically over the ferromagnetic element. This simplifies the interface logic by restricting current flow to a single direction on each wire, as opposed to requiring that the interface logic allow current to flow in both directions over a single wire. To avoid contention, the interface logic ensures that current flows through only one of the wires at a time.



**Fig. 3.** Interface logic for HHE reconfigurable gate with reset. Current in the left input wire may only flow downwards, while current in the right input wire may only flow upwards



**Fig. 4.** Interface logic for HHE reconfigurable gate with output feedback

Fig. 3 illustrates the interface logic for a 2-input HHE reconfigurable gate with two input wires. The right input line is used to reset the HHE gate output (and magnetization) to a default state. After this reset phase, the HHE gate is evaluated by enabling a pulse current through the left input line. Such HHE gates are analogous to dynamic digital CMOS circuits requiring a precharge/predischarge phase.

In this circuit, signals  $a$  and  $b$  are the inputs to the reconfigurable gate, while signal  $G0$  is a configuration signal that determines which function the gate will compute.  $G0$  is assumed to be the output of a bit of configuration memory, which may be implemented using another HHE device, as we will discuss later in the paper.

The sizes of transistors  $Ma$ ,  $Mb$ , and  $MG0$  are selected such that the current  $I_{in1}$  exceeds the switching threshold of the ferromagnetic element if two or more of the transistors are turned on during the time period when PULSE is high. (Transistor  $MP$  must also be sufficiently large to allow this current flow.) Thus, if  $G0$  is 0, the circuit will compute the logical AND of  $a$  and  $b$ , and, if  $G0$  is 1, the circuit will compute the logical OR of  $a$  and  $b$ . If external inverters and multiplexors are added so that the inputs  $a$  and  $b$  may be inverted under the control of another configuration input  $G1$ , it becomes possible to compute the AND, OR, NAND, and NOR of the inputs, with the potential to vary the computation being performed on a cycle-by-cycle basis. The circuit shown in Fig. 3 may also be extended to com-

pute functions of more than two inputs by adding additional transistors  $Mc$ ,  $Md$ , etc. in parallel with  $Ma$ ,  $Mb$ , and  $MG0$ , although this requires appropriate resizing of  $MG0$  and decreases the noise margins and tolerance of fabrication variations of the gate.

#### 4 HHE Reconfigurable gate with Output Feedback

The last section described a basic dynamic implementation of a HHE reconfigurable gate. Since power dissipation is a huge issue with current HHE and other magnetoelectronic devices, low-power circuit designs must be implemented. In this subsection, a static design is introduced that removes the power-hungry reset phase.

Previously, the HHE reconfigurable gate required a reset phase to place the magnetization into a known state. One issue with this methodology is that excess power is consumed in switching the magnetization to a default state even when the HHE output does not change between different input vectors. To reduce the power consumption of HHE gate operation, the reset phase must be eliminated altogether. Fig. 4 illustrates a design that removes the reset phase by incorporating output feedback.

Like the previous design, this circuit assumes a two-wire HHE gate, and is designed so that current flows unidirectionally through each of the wires. Instead of the reset line used in the previous circuit, this design incorporates dual pull-up and pull-down structures, which are gated by the PULSE signal to prevent static current flow and power consumption. In addition, the pull-down structure is gated by the output of the circuit (OUT) and the pull-up structure is gated by the inverse of the output (OUT') to ensure that no power is consumed on cycles when the output of the gate does not change.

To illustrate the operation of this gate, consider the case where the gate is configured to compute the OR of its inputs ( $G0 = 1$ ,  $G0' = 0$ ). Assume that the gate starts out with an output of 0, so that transistor  $Mout$  is off, and transistor  $Mout'$  is on. In this case, when the PULSE signal goes high, the current  $I_{in1}$  through the pull-up structure on the left half of the circuit will be sufficient to change the magnetization state of the ferromagnetic element if either  $a$  or  $b$  is 1, correctly computing the OR of these two inputs. Since the output of the gate starts at 0, no current flows through the pull-down structure in the right half of the figure, but this is acceptable because the ferromagnetic element will retain its state indefi-

nately. If the starting value of the gate's output had been 1, then no current would have flowed through the pull-up structure, and the current through the pull-down structure would only be sufficient to set the output of the gate to zero if both  $a'$  and  $b'$  were one, corresponding to inputs  $a$  and  $b$  both being zero.

Like the previous circuit, this circuit requires two configuration bits to implement the functions AND, OR, NAND, and NOR: a configuration bit  $G0$  to select between the AND/OR functions, and a configuration bit  $G1$  to control whether the inputs to the gate are inverted before the function is computed. Adding an input enable that allows one of the inputs to be forced to zero would further extend the functionality of the circuit, allowing it to be configured as either an inverter or a memory element.

HHE reconfigurable gates with input inversion and input enabling may be incorporated into non-volatile chips such as PLAs and CPLDs. Currently, EEPROM transistors are the underlying technology of these chips. EEPROMs are useful for realizing product terms with wide-AND operations commonly used in state machines and control logic. By replacing EEPROM transistors with HHE devices, there is more flexibility in realizing a particular function. A two-level AND-OR or two-level OR-AND implementation may be picked for the given function depending on which results in the fewest number of HHE gates used (i.e. fewest number of product/sum terms.) For complete non-volatile operation, the configuration bits for these HHE gates may be stored in non-volatile HHE LUT cells as described in section 6.

## 5 Threshold Logic Circuits

At the device physics level, the HHE is inherently a threshold-based device. Input currents above a certain magnitude set the magnetization direction of the device's ferromagnetic element, while currents below that magnitude do not. By adding additional transistors  $M_c$ ,  $M_d$ , etc. and additional configuration bits  $G_2$ ,  $G_3$ , etc. to the pull-up and pull-down structures, it is possible to design a HHE-based circuit that performs generic threshold-based computations (e.g. output = 1 if more than two of the inputs are 1.) Being able to implement generic threshold gates efficiently gives system designers interesting new options to work with, and we are currently investigating system designs that take advantage of threshold logic.

## 6 Non-volatile LUTs Using HHE Devices

Non-volatility is a key advantage of HHE devices. Having a non-volatile system is beneficial for "instant on" operation. In the case of FPGAs, configuration data will be immediately available once the system is on rather than loading configuration data from an outside source (configuration RAM, off-chip). "Instant on" operation is particularly important for control, military, and mobile applications. An HHE device may be incorporated to a standard LUT cell as shown in Fig. 5.

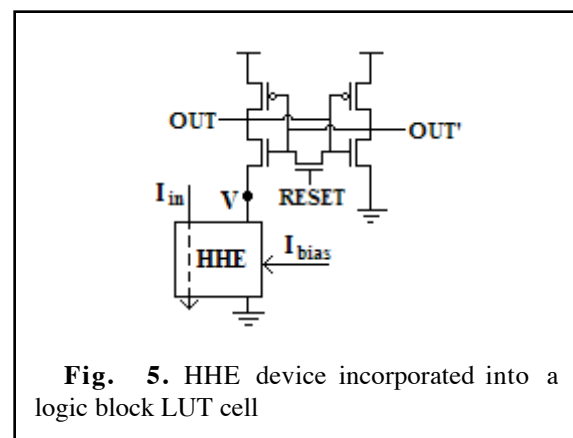
The HHE device in Fig. 5 has no fabrication offset; hence the output voltage levels are bipolar (positive/negative). To read information from the HHE device, the LUT cell requires a reset such that  $OUT$  and  $OUT'$  have no biased regeneration direction. After RESET is pulled low, the read bias current for the HHE device is turned on, and an HHE output voltage is created. The cross-coupled inverters act to regenerate the output signal of the HHE device to CMOS-compatible logic levels.

Although only a single HHE device is depicted in Fig. 5 one more may be added to the right leg of the LUT cell. In this manner, one of two configurations may be dynamically loaded into the LUT cell by applying the appropriate read bias current  $I_{bias}$  through the desired HHE device.

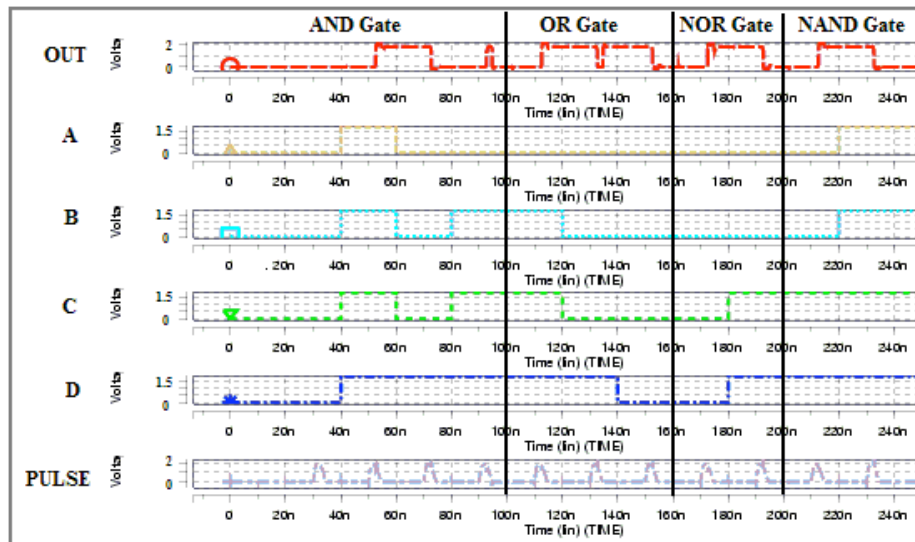
## 7 Simulation Results

To evaluate our circuit designs, we have implemented an HSPICETM model for the HHE device, based on the techniques presented in [2] and have simulated the circuits presented in this paper. The CMOS transistors used in these simulations were designed using parameters from a 0.18-micron fabrication process with a 1.8V power supply.

Fig. 6 illustrates the operation of a four-



**Fig. 5.** HHE device incorporated into a logic block LUT cell



**Fig.6.** Simulations for HHE reconfigurable gate

input reconfigurable gate with output feedback, similar to the design presented in Fig. 4. In this simulation, the configuration of the gate was varied to illustrate that it correctly computed different functions of its inputs, which were changed every 20ns. 10ns after each input change, the PULSE input to the gate was asserted, causing it to compute its outputs. One should note that these results are intended to illustrate functional correctness of the circuit, and not actual performance. In particular, the HHE device model used is based on very early prototype devices, and it is expected that performance of the devices will improve significantly as they are scaled to smaller sizes.

An interesting feature of these waveforms is the glitches on the circuit output at 92ns and 132ns. These occur when the PULSE input is asserted but the final output of the gate does not change, and reflect that current is flowing through one of the HHE device's input wires, but that the magnitude of the current is not sufficient to change the magnetization state of the device.

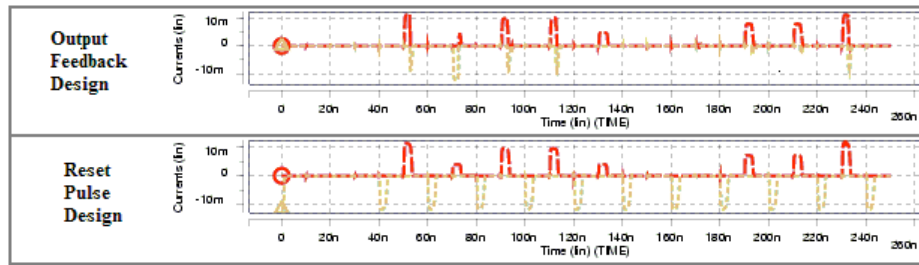
Fig. 7 shows the input current pulses on each of the HHE device's input wires when the input vectors from Fig. 6 are applied to four-input gates based on output feedback (Fig. 4) and reset pulse (Fig. 3) designs. The top curve in each waveform trace shows the current through the left (pull-up) input wire in each design, while the bottom curve shows the current through the right (pull-down) wire. Qualitatively, one can see that the reset pulse-based design requires significantly more and

larger current pulses on the pull-down input wire, because the magnetization state of the HHE device is set to zero at the start of each evaluation period, while the output feedback-based design only flows current along that wire when the output of the gate changes from one to zero. Similarly, the output feedback-based design requires less current on the pull-up input wire, because no current flows through this wire when the output of the gate remains one from cycle to cycle.

For the input waveforms found in Fig. 6, we found that the output feedback-based design consumed 2.4x less power than the reset pulse-based design (1.69mW vs. 4.09mW), although the energy savings will vary both as the dimensions of the HHE devices used change and with the activity factor of the circuit's output.

## 8 Conclusion

Hybrid Hall effect devices are an attractive implementation technology for non-volatile reconfigurable logic systems. In this paper, we have presented some early designs that illustrate the use of these devices to form reconfigurable circuits. Future work will develop larger-scale reconfigurable systems based around HHE devices, such as PLAs and FPGA-like systems. In addition, we are beginning a set of fabrication experiments that will demonstrate the correctness of our designs.



**Fig. 7.** Input current pulses for output feedback and reset pulse designs for two HHE reconfigurable gates. Top curves represent the current through the left HHE input wire. Bottom curves represent the current through the right HHE input wire

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