Abstract - Transient faults in logic circuits are an important reliability concern for future technology nodes. In order to guide the design process and the choice of circuit optimization techniques, it is important to accurately and efficiently model transient faults and their propagation through logic circuits, while evaluating the error rates resulting from transient faults. To this end, we give an overview of the existing formal methods for modeling and reasoning about transient faults. We describe the main aspects of transient fault propagation and the advantages and drawbacks of different approaches to modeling them.

Categories and Subject Descriptors: B.8.1 Reliability, Testing, and Fault-Tolerance

General Terms: Reliability

Keywords: SER, reliability, symbolic techniques

1. Introduction

Sensitivity of circuits to radiation faults has been an important topic of research starting from the seventies [13] through the mid nineties [32]. In recent years, increased technology scaling has resulted in devices and systems that are more sensitive to transient faults [18]: not only that the effect of radiation particles has increased, but also sources of transient faults have increased in their number. For example, current systems can contain many millions of gates, working at very high frequency and very small power supplies, therefore leading to increased cross talk or ground bounce, as well as the variant behavior of transistors.

Faults that are induced by radiation still receive most of the attention among transient faults and they are claimed to be one of the major challenges for future technology scaling [4]. A transient fault in a logic circuit, resulting from a single particle hit, is often referred to as a single-event transient (SET). An error caused by a transient fault is called soft error, due to the fact that if a failure results as the end effect of this fault, only data are destroyed. In contrast to this, hard errors stem from permanent or intermittent faults that result from the damage in the internal structure of semiconductor material. Another often used term for a radiation-induced error is single-event upset (SEU). In case of logic circuits, as stated recently [27][28], logic soft errors are more likely to contribute more to the global soft error rate (SER). This stems from the fact that fault masking is decreasing in logic, making it more susceptible to soft errors. Moreover, once a glitch can propagate freely through combinational circuit, sequential circuits will become very sensitive to such events [3].

A number of approaches were proposed in recent years to tackle the problem of evaluation of logic circuit susceptibility to transient faults. One obvious method is to inject the fault into the node of the circuit and simulate the circuit for different input vectors and for different fault originating locations (nodes), in order to find whether the fault propagates [32]. However, this approach becomes intractable for larger circuits and larger number of inputs and thus gives way to formal approaches that use analytical and symbolic methods to evaluate circuit susceptibility to transient faults.

The main goal of formal modeling of transient faults in logic is to allow for efficient estimation of the susceptibility of combinational and sequential circuits to transient faults, with a small estimation error. Although so far there have been several design solutions that address the transient fault issue, the remaining challenge (emphasized by technology scaling) is finding low cost solutions exhibiting best tradeoffs among power, performance, and cost on one hand, and reliability, on the other hand [9]. Reliability analysis is proven to be essential in early design stages for improving system lifetime and for allowing exploration of existing tradeoffs [2]. Therefore, fast and accurate estimation of error rates resulting from transient faults in logic circuits is crucial for identifying the features needed for future reliable circuits. In other words, these models can be used to reduce the cost of applying various techniques for error hardening, detection and correction.

The rest of this paper is organized as follows. In Section 2, we present the main aspects of transient fault propagation and modeling. In Section 3, we briefly describe and contrast different formal approaches. We discuss the importance of accuracy for circuit optimization in Section 4, while in Section 5, we tackle several other aspects of modeling faults in logic circuits: sequential circuit case, impact of process variations and multiple simultaneous faults. We conclude our discussion of formal methods for reliability analysis with Section 6.

2. Fault modeling in logic

We describe in the following the elements of modeling transient faults in logic that are related to individual nodes in the circuit and a very important aspect of transient fault modeling in logic circuits - the set of masking factors (logical, electrical and latching-window masking) that can prevent the fault from propagating to the outputs of the circuit. Finally, we discuss modeling of reconvergent glitches.

2.1. Transient fault shape

When evaluating the impact of transient faults on circuit reliability, before developing a model for transient fault propagation, one first needs to make a decision about the pulse shape. In other words, it is necessary to determine which parameters will be used to describe a pulse that represents a transient fault. One approach to modeling pulses is to use a very accurate model, which requires more information about the glitch (e.g., the current pulse that results from a particle strike can be described as a double exponential function). However, there is a tradeoff between the accuracy of the glitch model and the efficiency of associated modeling methodologies for the impact of the glitch on circuit outputs. Another possibility is to model the pulse as piecewise linear and, in that case, it is enough to represent the pulse using a number of parameters. Simpler models, like triangular or trapezoidal [1][6][14][21] include information about glitch duration only, amplitude only, duration and amplitude, and some models include the slope in addition to duration and amplitude [21].

2.2. Logical masking

When the transient fault arrives at the input of a gate inside the circuit under consideration, if at least one of the other inputs of that
gate has a controlling value, the fault is logically masked. In other words, this prevents the fault from propagating through the gate and consequently, prevents the fault from propagating further through the circuit, to the memory element at the end of the path. When analyzing single gates, without taking into account the surrounding context, the sensitivity of a gate to the input fault depends on the type of gate and values at the unaffected inputs. From a more global (circuit) perspective, values at gate inputs depend on the values at primary circuit inputs. Therefore, most modeling approaches keep track of signal values [14][25][30][29] (or probabilities [2][5][10]) starting from primary inputs and compute signal values (probabilities) at each gate output. These signal values (probabilities) are then used to compute propagated fault probability in a fanout cone of a gate where the fault originated.

2.3. Electrical masking - pulse attenuation

Due to the relation between electrical properties of gates and the size of the pulse representing the transient fault, the fault may be attenuated (electrically masked) by the gates through which it propagates. Thus, electrical masking depends on the properties of the gate the fault propagates through, as well as on the properties of the fault (e.g., duration and amplitude) that resulted from the initial characteristics of the fault and the path it propagated through. There is a number of methods that do not model electrical masking, and instead just focus on logical masking [5][7][8][10] and, in some cases, on latching-window (timing) masking (described in Section 2.4) [2][5][7][8][10]. However, approaches that completely overlook electrical masking and simplify modeling by assuming logical and latching-window masking only, are unable to estimate the magnitude of error masking due to electrical effects, and thus provide too pessimistic error rate values, in many cases overestimated by more than a factor of 3X. As it can be seen in Figure 1, in most cases, logical masking has approximately the same impact as electrical masking in affecting the propagated glitch, therefore emphasizing the importance of considering electrical masking impact. Furthermore, as described in more detail in Section 5.2, the impact of process variations on error rates is increasing. Approaches that tackle the electrical masking effects, rely on one of two main approaches: (i) Lookup table-based [21][22][24]; and (ii) Analytical modeling [14][19]. In both cases, there is a tradeoff between accuracy and efficiency, and often, this is the main source of error. To find the balance between accuracy and efficiency, it is possible to use a hybrid approach based on the combination of the two; for example, lookup table for pre-characterization of some of the parameters of gates in the library and analytical modeling for computing propagated pulse duration and amplitude [14][21].

2.4. Latching-window (timing) masking

When the transient fault arrives to the input of a memory element, it will be latched only if it arrives on time to satisfy setup and hold time conditions. In other words, if, for example, the pulse arriving to the input of a flip-flop represents a 0-1-0 transition, then its rising edge needs to reach the threshold level of a flip-flop (or latch), at least a setup time before the clock edge, and its falling edge needs to reach the threshold level of a flip-flop at the earliest a hold time after the clock edge. In order to determine the probability of timing masking, one needs to compute (i) the interval during which the pulse is allowed to occur; and (ii) the interval during which the pulse needs to occur in order to be latched.

The propagation of the glitch and the glitch parameters of interest (duration and amplitude) when latching-window (timing) masking is considered, are presented in [14]. The latching of a glitch may also depend on the slope of the rising and falling edge of the glitch. The impact of amplitude and slope on latching-window masking is taken into account in [21], by pre-characterizing flip-flops and using a lookup table to determine whether a glitch with given duration, amplitude and slope is latched. If the impact of amplitude and the slope is approximated analytically under conservative assumptions, the computed output error probability [14] is also a conservative upper bound of the exact values. The evaluation of the impact of latching-window masking must take into account both local properties (setup and hold time of the flip-flop), and global properties (the pulse characteristics – arrival time, duration amplitude and slope) that resulted from its propagation through the circuit. However, most of the formal approaches that were proposed thus far include only a subset of these parameters in order to tradeoff accuracy for efficiency [11][21][14][1][6].

2.5. Reconvergent glitches

Once a transient fault occurs at the output of a gate within the circuit, it may propagate through the circuit on more than one path. Besides affecting multiple outputs of the circuit, glitches propagating on different paths can result in reconvergent glitches at different inputs of the same gate in the fanout cone of the original gate.

In Figure 2(a), an example benchmark circuit, S27, is shown, with its reconvergent paths highlighted. In circuit S27, there are two paths from gate G1, that reconverge at gate G2, and thus affect the probability of error propagation to the output of the circuit and two next-state lines. From gate G1, there is one path leading directly to gate G2 and one that goes through gate G3 creating overall three possible reconvergent paths to one of the next-state lines and two reconvergent paths to the output and another next-state line. As will be described in Section 3.1, it is important to model reconvergent glitches when modeling glitch propagation. Methods that do not model reconvergence can incur a significant error when estimating circuit reliability. However, as will be shown next, only approaches that simultaneously model logical and electrical masking are able to accurately incorporate reconvergent glitch modeling [14][21][29]. Furthermore, only those methods that keep track of the exact signal values at the reconvergence site can model the correlation of gate inputs accurately [14][29], while methods that only propagate signal probabilities can only approximate input correlations [1][5][6].

3. Fault propagation modeling methodology

We provide in this section a comparison of different methodologies that have been proposed for evaluating circuit susceptibility to transient faults.
Different initial glitch sizes.

A fault propagating from a given gate (fault source) to a given output either propagates on a single path, or it propagates on multiple paths that reconverge before reaching the output. Reconvergent paths for circuit $S27$ are highlighted in Figure 2(a). In the former case, since the size of the glitch at the output is the same for all input vectors that allow glitch propagation, then the logical masking probability can be summed across all these input vectors and multiplied by the probability of latching the glitch with the computed size. Therefore the computed probability is same for both separate and unified approach. In the latter case, when more than one path exists from a given gate to a given output, one needs to analyze two possible sub-cases: (a) glitches on some of the paths are attenuated before reaching the reconvergence point and (b) glitches on all paths are propagated to the reconvergence point, where they merge into the resulting glitch(es) with new durations. In these two different sub-cases, the separate computation of different masking factors will incur an error, since it sums separately (i) probabilities of sensitization of all reconvergent paths, and (ii) probabilities of latching on all reconvergent paths; and then it multiplies the two terms.

The significant difference in error probability evaluation between a unified approach and separate approaches can be seen from the results presented in Figure 2(b). The left table of Figure 2(b) presents results for circuit $C17$, for three different input vector probability distributions. The right table of Figure 2(b) represents minimum, maximum and average relative error of the model that evaluates electrical, latching-window and logical masking separately, compared to the unified model averaged across ten different input vector probability distributions, for three different initial glitch durations. All results are computed using the framework from [14],[16] which has been validated against HSPICE. As it can be seen, merely computing independently and multiplying the logical masking and electrical/latching-window masking probabilities leads to a huge error in the probability of latching the glitch, which can be as large as 3100%. However, for smaller glitch duration (80ps), the average error is not very large, due to the fact that most glitches are electrically masked, and therefore, separate and unified methods give similar results. For the case of large initial glitches (125ps), all glitches propagate, the only difference being the way reconvergent paths are handled.

### 3.2. Symbolic modeling approach

Most of the previous approaches either treat a subset of masking factors [2],[5],[8],[10],[19], or treat and evaluate their impact separately and then merge them into the final reliability measure [6],[25],[30],[31]. However, as seen from the above discussion and the examples in Figure 2, treating logical, electrical and latching-window masking in a unified manner is mandatory for highly accurate estimations, and only the unified method can take into account the fact that:

- The propagation of a glitch depends on inputs and circuit topology since, for different input vectors, different paths in the circuit are sensitized;
- Glitch attenuation from the originating gate to circuit outputs depends on the gates through which glitch propagates, and thus, it has to be considered synergistically with logical masking;
- The probability of latching the glitch depends on the glitch size at the output, which in turn is a function of: the initial size of the glitch and the attenuation on the sensitized paths and the size and relative arrival time of reconvergent glitches, which affects the amplitude and duration of the resulting glitch.

One approach that is able to treat the three masking factors in unified manner is proposed in [14]. The main idea is that the impact of the three masking factors can be modeled using Binary Decision Diagrams (BDDs) and Algebraic Decision Diagrams (ADDs). The sensitization on glitch propagation paths is represented using BDDs, while the size of the glitch is represented using ADDs. Non-terminal nodes in both BDDs and ADDs represent primary input variables and terminal nodes represent logical sensitization in BDDs and glitch size in ADDs. This approach is explained in more detail in [14]. In Figure 3(a)(right), we give an example of glitch duration ADDs and sensitization BDDs generated for benchmark circuit $C17$ (Figure 3(a)(left)), assuming that a glitch originates at gate $G_3$ and propagates through gates $G_4$ and $G_5$, to primary output $F$. The ADD computed for the glitch at the output of gate $G_3$ represents the duration (amplitude) of the glitch propagated from gate $G_3$ to primary output $F$. This example shows the propagation of one glitch only. However, the important advantage of the model proposed in [14] is...
that it concurrently computes the propagation and the impact of transient faults originating at different internal gates of the circuit. A similar approach has been proposed in [29], but it uses BDDs only and the algorithm presented is run separately for different polarities at the output of affected gate (fault source location) and separately for each affected gate. The concurrent computation of glitch propagation can account for both single faults and multiple simultaneous faults (explained in more detail in Section 5.3).

3.3. Pre- vs. post-layout modeling

Formal models that target transient faults most often assume that the layout information is not yet available and do not rely on any such information. Such an approach allows for more flexibility in using these methods, as they can be applied in early design stages, when no layout data is available. The necessity and importance of layout information can be discussed from the perspective of modeling masking effects. In case of logical masking, the information necessary for modeling is the circuit netlist and input vectors and therefore, unaffected by physical design information. For electrical masking, one needs to have data about electrical properties of gates, and interconnect or layout information is largely irrelevant while pre-characterizing electrical masking properties of gates. As already discussed in Section 2.3, the more parameters are used for modeling attenuation, the more accurate the model is, but often with high impact on complexity and efficiency. The only component affected by physical design is timing masking, since arrival time of faults to outputs are important to keep track of; this indeed requires knowledge about delays on paths from the fault source to outputs, which does depend on layout information. However, as described in Section 2.4, most modeling methodologies use conservative assumptions and compute timing masking with respect to the worst-case scenario. One such example is presented in [14], where a maximum delay constraint is used when computing the latching window masking to determine a conservative upper bound for the SER (within 4% of the exact values). Similar to the case of electrical masking, when more parameters are included, runtimes are longer, but the precision is better.

Therefore, relying on layout information may provide modeling techniques with more accuracy, but at the same time will limit them to an already refined, post-layout and therefore, less amenable to design changes. Very often, designers prefer to have reliability estimates early in the design process to be able to reason about applying necessary optimization and protection techniques. This emphasizes the importance of highly accurate, conservative, modeling techniques that do not strictly require layout information.

3.4. Error rate computation

In order to find error rates at primary outputs and global error rates for a given circuit, one needs to have information about (i) fault sources; (ii) the rate of occurrence of faults; and (iii) the likelihood for different parts of the circuit to be affected by SETs. Next, one needs to have an efficient and accurate modeling methodology to capture the propagation of faults to outputs and to estimate the output error probability. In general, parameters that are specific for individual fault types and sources (e.g., magnitude, occurrence rate) should not be incorporated into the model, but instead should be inputs to or parameters for the model.

To find the overall circuit error susceptibility, one can average across all output error probabilities or find the maximum and minimum output error susceptibility. However, multiple errors can occur as a result of a single fault being propagated and latched by more than one flip-flop or memory cell [15]. Multiple latched faults are of special concern in sequential circuits where, if latched by state flip-flops, they can continue to propagate through the circuit, causing errors in more than one clock cycle. In addition, averaging across output error probability to determine mean susceptibility of a circuit to faults may introduce additional errors, if output error correlations are not accounted for. The reliability of a given circuit when all output correlations are known, can be found using output error probabilities:

\[
R = 1 - \left( \sum P(F_j) - \sum P(F_j \cap F_k) + \sum \sum P(F_{j_k} \cap F_{j_l} \cap F_{j_m}) - \ldots + \sum \sum \sum \sum P(\bigcap F_{j_{n}}) \right)
\]

where \( n_p \) is the number of primary outputs, \( P(F_j) \) is the probability that outputs \( F_1, \ldots, F_n \) have latched errors in the same cycle, stemming from the same fault source.

However, taking into account all possible output correlations can produce an inordinate increase in complexity. One can instead determine upper and lower bounds for circuit error probability, by computing correlations across pairs or triplets of outputs only. The symbolic approach that uses BDDs and ADDs is very convenient for determining these correlations, since ADDs that represent glitches at circuit outputs include the information about all input vectors and finding output error correlations requires only multiplication of these ADDs (that is, AND-ing of their corresponding BDDs).

3.5. Scalability of symbolic techniques

The techniques proposed thus far for modeling of transient fault propagation, most often suffer from the scalability issue. Some techniques require extraction of all paths from a given gate to all circuit outputs from the circuit and then traversal of each path subset separately to compute the impact of SETs on output errors. Obviously, this approach scales with the number of paths in the circuit, which may become too large. On the other hand, some
approaches traverse the topologically sorted list of circuits, but in each pass assume only one input vector. This approach again becomes intractable as the number of input vectors scale exponentially with number of inputs. One option is to analyze the circuit for a subset of input vectors, but this adversely affects the accuracy of the method.

When BDDs [14][29] and/or ADDs [14] are used to represent Boolean functions, there exist some limitations in terms of the complexity of algorithms used and the size of diagrams that are created during program runtime. One possible approach to improve the scalability of framework that relies on BDDs and ADDs is circuit partitioning [14][29]. The idea behind this approach is to partition gates of the circuit among several regions, such that, for example, the number of gates allowed in each partition is below a certain limit and/or the number of nets crossing the cuts between partitions is minimized. However, while allowing for partitions to be run separately, it is necessary to find the mechanism to combine the results from partitions, without a significant loss in accuracy (for example, by using the output statistics for one partition as input vector statistics for another partition they feed into). BDDs and ADDs represent a very convenient approach that can also be used to model input vector correlations and thus, could be applied to accurately model and evaluate error probability at outputs of individual partitions as well as the primary circuit output error probabilities.

4. Modeling accuracy and circuit optimization

Once the gate-output error probability, that is, the probability that a fault originating at the gate results in an error at the output, is obtained, it can be further used to obtain more information about the circuit. For each gate, one can find the fanout cone affected by the fault originating at that gate. Next, minimum, maximum, mean and median probability of error at outputs can be determined, given that the fault occurred at the specified gate. These values describe individual gate error impact and provide guidance for deciding which gates in the circuit need to be hardened. Similarly, for each output, a fanin cone can be found, representing all gates from which faults propagate to the output affecting its correctness. Minimum, maximum, mean and median probability of error at the given output can be computed, in order to better describe output error susceptibility. An input vector probability distribution provides an insight into how input patterns affect gate error impact and output error susceptibility. One can obtain information about circuit’s susceptibility to faults by computing the weighted average of error probability across different input probabilities.

The impact of latching-window masking may also vary across different circuits due to the initial size of the glitch, and the logical and electrical masking effects in the circuit. As seen in Figure 3(b), the increase in the size of latching-window did not affect much benchmarks 5xp1, s27 and z4ml. However, for 9symml, the reliability is initially very small, and thus latching-window size has more impact on it. Based on these results, we can draw conclusions about which parts of a specific circuit contribute more to transient fault masking, and which masking factors have more impact on fault propagation. Thus, based on such information (e.g., Figure 1 and Figure 3(b)), one can decide which techniques, or combination thereof should be used to obtain best results. For example, in case of circuit 9symml (Figure 1), improving electrical masking can lead to significant improvement in error rates.

Thus, in order to guide protection techniques, accurate modeling and evaluation of circuit reliability (error probability) is crucial. With the inclusion of power and performance data, the accurate model can be incorporated into the circuit design and optimization cycle, thereby providing power, performance, cost and reliability tradeoffs for different circuit implementations in earlier design stages. Underestimation that might occur due to neglecting the impact of variability or, in some cases, due to inaccurate modeling of reconvergence may result in inadequate protection or hardening choices. On the other hand, grossly overestimating error rates that can occur due to ignoring electrical and timing masking effects results in overly conservative protection and hardening techniques, and consequently, in overdesigning with higher performance penalty, power or area cost.

5. Other modeling aspects

In this section, we present other important aspects of fault modeling in logic circuits that did not have much attention until recently, and only a few approaches have been proposed to tackle them. First, we present modeling of faults in sequential circuits, then we give an overview of methods that include impact of process variations when computing error rates and finally, we describe the importance of modeling multiple simultaneous faults, which incidence increases with scaling.

5.1. Fault modeling in sequential circuits

While in case of logic circuits one pass through the circuit is enough to evaluate its susceptibility to given particle hit, in the case of sequential circuits this evaluation becomes much more difficult. Since sequential circuits have a feedback loop leading back to the state inputs of the circuit, it is possible that errors latched at state lines propagate through the circuit more than once and affect outputs during several clock cycles.

In the case of soft errors, the transient behavior of the circuit is more important than its steady-state, as used for other purposes, such as power analysis [12]. More specifically, one needs to determine: (i) the time the circuit spends transitioning through erroneous states until it reaches a steady-state behavior; and (ii) the effect this transitioning has on the outputs, that is, the susceptibility to soft errors of the target sequential circuit. One method that evaluates the probability of latching the error in sequential circuit in the cycles following the particle hit was proposed in [2]. In that work, the authors assume hits can happen at state flip-flops only and then, based on this information, find the error probability at each output due to each individual flip-flop hit. This analysis excludes cases where internal gates of circuit’s combinational logic are hit and do not include effects of electrical and timing masking.

In [16], a symbolic modeling approach is presented that estimates the probability of errors in sequential circuits in an efficient manner that captures both transient and steady-state effects, while easily incorporating the joint impact of logical, electrical, and latching window masking. The main idea is to use unrolling of the sequential circuit, in conjunction with symbolic modeling that relies on BDDs and ADDs. This approach allows for both accurate and efficient modeling of transient faults in sequential circuits in several cycles following the cycle when the fault occurred, and it also allows for analysis of the impact of both internal gates and state flip-flops on output error probability and overall circuit susceptibility.

5.2. Process variation-aware fault modeling

When considering transient faults and their impact on circuit reliability, it is important to take into account the fact that the delay of a particular gate is no longer constant across dies or within the same die, but instead should be characterized by a probability distribution. Variations in gate delays can affect the propagation of the glitch through the circuit, that is, its attenuation, and therefore, the circuit error rate [23]. With respect to modeling transient faults,
just a few approaches have been proposed thus far that included the impact of process variations. In [23], custom designed circuits were simulated using HSPICE. The benchmark circuits considered by the authors were analyzed by running separate simulations for each discrete parameter value. In [17], an efficient modeling of transient fault propagation in logic circuits is proposed that includes simultaneous variation of several process parameters. Gate delay and output glitch duration and amplitude are modeled explicitly as functions of process parameters in [17], and transient fault propagation is modeled using a non-simulative, symbolic approach that is orders of magnitude faster than HSPICE simulation [14]. As can be seen from results presented in [17], the nominal case can incur an error in the evaluation of circuit susceptibility to transient faults and thus lead to non-optimal design decisions. The claim that using static analysis, without taking into account process variations can underestimate error rate estimation is further confirmed with experimental results recently presented in [20].

5.3. Multiple fault modeling

Future technology nodes are expected to face increased rate of multiple transient faults [15], stemming from either single events, such as a radiation hit, or different, but simultaneous multiple events, such as crosstalk, ground bounce, IR drop or radiation [31]. The problem of the impact of multiple transient faults occurring simultaneously has been addressed in the past, but it focused mostly on their effect in memories, in the light of the multiple upsets resulting from a single transient phenomenon. Until recently, multiple transient faults in logic received very little attention, due to their rare occurrence. These trends are changing [15], therefore making modeling and analysis of multiple faults as important as modeling and analysis of single faults. Similar to single transient faults, previous work that focused on multiple faults in logic circuits used, to the best of our knowledge, only simulation. Several symbolic approaches described before could model multiple faults, but they only assumed logical masking [5][10]. As described in Section 3.1, it is very important to include all three masking factors and model them in a unified manner, in order to achieve highly accurate estimates. A formal approach that uses symbolic techniques for modeling multiple faults and accounts for the impact of all three masking factors was presented in [15].

6. Conclusion

We presented in this paper the aspects of transient fault propagation that need to be accounted for when using formal methods to model and analyze them. In addition, we gave an overview of how these aspects have been tackled by different symbolic and analytical approaches proposed thus far. We also described the important elements of analysis of transient faults in sequential circuits, impact of process parameter variability and the elements of modeling multiple faults. Finally, we discussed the importance of accurate and efficient modeling for the purpose of guiding the design process.

7. References


