ProtoFlex: An Architectural Exploration Vehicle using FPGA-Accelerated, Full-System Multiprocessor Simulation

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Intended audience: academic/industrial researchers interested in learning about and using FPGA-based simulators to perform fast architectural exploration

Abstract

This half-day tutorial will introduce participants to the ProtoFlex simulation architecture and development flow. ProtoFlex is an FPGA-accelerated platform for fast architectural full-system simulation of multiprocessors. Using commodity FPGA platforms, the ProtoFlex Simulator models the architectural behavior of a 16-CPU UltraSPARC III SMP Server and can execute unmodified, commercial applications in Solaris. Performance-wise, the ProtoFlex Simulator achieves a 10-100X speedup over equivalent software-based architectural simulation when trace-based instrumentation is enabled.

In the first part of this tutorial, we will cover the high-level virtualization concepts used to develop the ProtoFlex Simulator. This includes the *hybrid simulation* concept that enables full ISA compliance without undue development effort and *host multithreading*, in which multiple logical processors share the resources of a fewer number of multithreaded FPGA cores.

In the second part of the tutorial, participants will be given the opportunity to build a complete design from scratch that runs on FPGA hardware (specifically, the XUPV5-LX110T platform). In addition, participants will perform the steps needed to prepare and stage multithreaded workloads for simulation on the FPGA. Key concepts such as RTL modification, instrumentation, debugging, and validation will be covered. In addition, all of the required equipment and source code will be provided at the tutorial. Participants will only need to bring a laptop.

For more information, please visit http://www.ece.cmu.edu/~protoflex.