Fast Flexible FPGA-Tuned Networks-on-Chip
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Networks-on-Chip (NoCs) and FPGAs
- Rapid growth of FPGA capacity & features
  - Extended SoC and full-system prototyping
  - FPGA-based high-performance computing
- Need for flexible NoCs to support communication
- Map existing ASIC-oriented NoC designs on FPGAs?
  - Inefficient use of FPGA resources
  - ASIC-driven NoC arch. not optimal for FPGA
- CONNECT FPGA-tuned NoC Architecture
  - Embodies FPGA-motivated design principles
  - Very lightweight, minimizes resource usage
  - Publicly released flexible NoC generator

The CONNECT NoC Architecture
- FPGAs peculiar HW realization substrate
  - Relative cost of speed vs. logic vs. wires vs. mem.
  - Unique mapping and operating characteristics
- CONNECT focuses on 4 FPGA characteristics:
  1. Abundance of Wires
  2. Storage Shortage & Peculiarities
  3. Frequency Challenged
  4. Reconfigurable Nature
- FPGA characteristics uniquely influence NoC design decisions, which often go against ASIC-driven NoC conventional wisdom.

CONNECT vs. ASIC-Oriented RTL
- 16-node 4x4 Mesh Network-on-Chip (NoC)
  - SATA: state-of-the-art high-quality ASIC-oriented RTL
  - CONNECT: identical config. with generated RTL
- FPGA Resource Usage
  - (same NoC configuration)
  - Network Performance (uniform random traffic @ 100MHz)

CONNECT Architecture
- CONNECT Router
  - Input Ports
    - In0 (flits)
    - In0 (mem)
    - In0 (send)
  - Output Ports
    - Out0 (flits)
    - Out1 (flits)
    - Out2 (flits)
    - Out3 (flits)
- Switch
  - Arbiter & Flow Control State

CONNECT Network Examples and Results
- Four sample CONNECT Networks (router, endpoint)
  - 16 endpoints, 2/4 virtual channels, 128-bit datamap
- All above networks are interchangeable from user perspective.

FPGA Synthesis Results
Network
<table>
<thead>
<tr>
<th>Network Configuration</th>
<th>Synthesis Results</th>
</tr>
</thead>
<tbody>
<tr>
<td># Routers</td>
<td># VCs</td>
</tr>
<tr>
<td>Ring</td>
<td>16</td>
</tr>
<tr>
<td>Fat Tree</td>
<td>20</td>
</tr>
<tr>
<td>Mesh</td>
<td>16</td>
</tr>
<tr>
<td>High Radix</td>
<td>8</td>
</tr>
</tbody>
</table>
* 10% LUT utilization for all networks, No Block RAMs

CONNECT NoC Generator Public Release
- NoC Generator with web-based interface
  - Supports multiple pre-configured topologies
  - Includes graphical custom topology editor
  - Some Release Stats (since release in March 2012)
    - 200+ unique visitors
    - 200+ network generation requests

Conclusions & Public Release
- Significant gains from tuning for FPGA
  - FPGAs and ASICs have different design “sweet spot”
- Compared to ASIC-driven NoCs, CONNECT offers
  - Significantly lower network latency and
  - ~50% lower LUT usage or 3-4x higher network performance
- Take advantage of reconfigurable nature of FPGA
  - Tailor NoC to specific communication needs of application

CONNECT NoC Generator Public Release
- http://www.ece.cmu.edu/~mpapamic/connect

Please see our FPGA 2012 paper for more synthesis and performance results.