Personal

Date of Birth: July 5, 1983
Citizenship: United States of America
Languages: Fluent in English, Greek and German

Contact Information

Address: 5000 Forbes Ave.
Pittsburgh, PA 15213
U.S.A.

Phone: +1 (412) 268-9388
Cell: +1 (412) 973-2662
E-mail: papamix@cs.cmu.edu or papamix@gmail.com
Homepage: http://www.cs.cmu.edu/~mpapamic

Education

PhD
September 2007 - Present
Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA (http://www.cs.cmu.edu)

Thesis Title: Pandora: A Knowledge-Encapsulating IP Development Paradigm to Overcome the Complexity Wall in Hardware Design

Research Areas: On-chip interconnects, reconfigurable architectures, hardware acceleration, IP design methodologies, scheduling in multi-core environments

Advisor: Prof. James C. Hoe (http://www.ece.cmu.edu/~jhoe)

Master of Science
July 2007
Computer Science Department, University of Crete, Heraklion Crete, Greece (http://www.csd.uoc.gr)

Major: Architecture of Microelectronic Systems
Minor: Parallel and Distributed Systems
Thesis Title: Network Interface Architecture and Prototyping for Chip and Cluster Multiprocessors

GPA: 9.78 out of 10 ("excellent") – *ranked first among all graduate students of the department*
Advisor: Prof. Manolis Katevenis (http://www.ics.forth.gr/~kateveni)

Computer Science Diploma
2005
Computer Science Department, University of Crete, Heraklion Crete, Greece (http://www.csd.uoc.gr)

Four-year professional degree program, equivalent to Bachelor of Science.

Diploma Thesis Title: SRAM Multiple Access Controller & Related Subsystems for a High-speed Network Interface Card

GPA: 8.78 out of 10 ("excellent") – *ranked second in class*
Diploma Thesis Advisor: Prof. Manolis Katevenis (http://www.ics.forth.gr/~kateveni)

Research Experience

PhD Candidate
2007-Present

Computer Architecture Lab at Carnegie Mellon (CALCM), Carnegie Mellon University, Pittsburgh PA, USA (http://www.ece.cmu.edu/calcm)

Pandora
2013-Present

The Pandora project argues for a new design paradigm for generator-based hardware IPs that encapsulates the IP authors' knowledge to assist the IP users' interactions with the IP. Under Pandora, an IP not only captures the microarchitectural or structural view of a hardware design, but also includes (1) characterization metadata; (2) high-level configuration and tuning interfaces that are tailored to the specific usage domain and are meaningful to the IP user; and (3) domain-aware simulation-time and run-time monitoring and introspection mechanisms. In addition to reducing complexity and boosting productivity, this new IP paradigm also dramatically reduces the combined total design effort because work that would otherwise be repeated by each IP user is now only performed once by the IP author.

As the lead student in the Pandora project, I have 1) developed **DELPHI** (see below) for performing fast and efficient IP characterization (power, area, frequency) across multiple technology nodes, 2) developed and evaluated **Nautilus** (see below), which uses modified genetic algorithms that incorporate IP author knowledge to accelerate IP optimization through automated guided design space search, 3) developed a set of hardware instrumentation components in both Bluespec System Verilog and Verilog, which is scheduled for public release, and 4) extended the **CONNECT** Network-on-Chip generator (see below) to demonstrate many of the Pandora design principles.

Nautilus
2014-Present

Nautilus builds on top of DELPHI to help IP users perform parameter optimization and navigate an IP's design space in a fast and automated manner. As the lead student in this project I developed a modified genetic algorithm that allows embedding of IP-author knowledge pertaining to the IP design space. This knowledge, coming in the form of "hints", captures the IP author's intuition about how IP parameters relate to the various metrics of interest; the goal is to help steer the optimization search process more quickly toward profitable regions or directions of the designs space. Our evaluation across multiple IPs show that author-guided instances of Nautilus can achieve the same quality of results up to an order of magnitude faster than a baseline genetic algorithm.

DELPHI
2014-Present

As the lead student in this project I developed a flexible, open framework that leverages the DSENT modeling engine (http://sites.google.com/site/mitdsent/) for fast, easy, efficient characterization of RTL hardware designs. The DELPHI flow processes Verilog or VHDL RTL hardware descriptions to generate a technology-independent DSENT design model, which can then be used to perform very fast—one to two orders of magnitude faster than full RTL synthesis—estimation of hardware performance characteristics, such as frequency, area, and power. The full DELPHI framework (including a fully open-source flow) will soon be available for download or for use through a web-based portal.

CONNECT
2012-Present

As the lead student in this project I proposed a new Network-on-Chip (NoC) architecture specifically tailored for FPGA implementation. To support this research, I developed and publicly released CONNECT (http://www.ece.cmu.edu/~mpapmic/connect), an NoC generator that can produce synthesizable RTL designs of FPGA-tuned multi-node NoCs of arbitrary topology. The CONNECT NoC architecture embodies a set of FPGA-motivated design principles that uniquely influence key NoC design decisions, such as topology, link width, router pipeline depth, network buffer sizing, and flow control, and in many cases go against conventional wisdom stemming from traditional ASIC-oriented NoC designs. A custom interconnect generator based on CONNECT is used as the main interconnection network within the CoRAM project (see below).

CoRAM
2012-Present

The CoRAM project (http://www.ece.cmu.edu/~coram) is an endeavor to standardize and simplify how FPGA computing applications interact with memory and I/O, which is a critical step towards building a portable FPGA abstraction. I have worked on multiple aspects of CoRAM, including 1) developing its custom interconnection network generator and 2) co-developing the Shrinkwrap framework, which was used to experiment with compiler-guided generation of application-specific Networks-on-Chip within the CoRAM FPGA memory abstraction. Compared to using a baseline generic interconnect, across a number of CoRAM application instances, Shrinkwrap's customized interconnects reduce FPGA resource usage by almost an order of magnitude, while retaining the same level of application performance.

FIST
2010-2011

As the lead student in this project I developed a set of fast, lightweight, FPGA-friendly Network-on-Chip (NoC) models that closely capture the behavior of time-consuming detailed NoC models in full-system performance simulators. Work included extending a full-system simulator to support and evaluate FIST software-based NoC models, as well as developing hardware in Bluespec System Verilog to experiment with FPGA-accelerated FIST models.

Thread Cluster Memory (TCM) Scheduling
2010

In this project I co-developed a new memory scheduler that exploits differences in the memory behavior of threads to maximize system throughput and fairness. Our MICRO paper on TCM was selected as one of IEEE Micro's 2010 Top Picks.

ProtoFlex
2007-2009

For the purposes of the ProtoFlex project (http://www.ece.cmu.edu/~protoflex) I designed and implemented FPGA-accelerated instrumentation components to achieve faster full-system high-fidelity computer architecture simulations. Instrumentation examples include:

- A functional model of a Piranha-like CMP cache hierarchy (in Verilog)
- A model of 2-level CMP Branch Predictor (in Bluespec System Verilog)

Research Intern at Intel Labs
July 2010-November 2010

Microarchitecture Research Lab (MRL), Intel Labs, Santa Clara, CA, USA
(http://techresearch.intel.com)

Worked on uncore hardware development and modeling for emerging multi-core systems. (details under NDA)

Mentor: Dr. Graham Schelle
Supervisor: Dr. Hong Wang, Intel Fellow (http://www.intel.com/newsroom/assets/bio/Fellows.htm)

Graduate Student Research Assistant
2005-2007

Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece (http://www.ics.forth.gr/carv)

Design and implementation of a network interface with multiple DRAM-resident queue support for use in the FPGA-based prototyping platform of the CARV laboratory for the purposes of the SARC project. (http://www.sarc-ip.org)

Supervisor: Prof. Manolis Katevenis (http://www.ics.forth.gr/~kateveni)

Student Research Assistant
2004-2005

Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece (http://www.ics.forth.gr/carv)

Design and implementation of an SRAM multiple access controller and other related subsystems for use in the high-speed network interface card in the FPGA-based prototyping platform of the CARV laboratory for the purposes of the cross-European project SIVSS. (http://www.sivss.org).

Supervisor: Prof. Manolis Katevenis (http://www.ics.forth.gr/~kateveni)

Student Research Assistant
2001-2004

Institute of Applied and Computational Mathematics (IACM), Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece (http://www.iacm.forth.gr)

Lead Software Developer in the “OASA” project for the Extension of the GIS system of the Athens Urban Transport Organization.
(http://www.iacm.forth.gr/regional/projects/auto-gis.html)

Manipulation and enrichment of vector maps with GIS data for the company Infocharta.
(http://www.infocharta.gr/)

Supervisor: Dr. Poulicos Prastakos (http://www.iacm.forth.gr/regional/people/prastakos.html)

Teaching Experience

Guest Lecturer

Spring 2014 *Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*
Guest Lecture on "Interconnection Networks" for the undergraduate Computer Science **15-418/15-618 Parallel Computer Architecture and Programming** course (http://15418.courses.cs.cmu.edu/), March 24, 2014

Fall 2013 *ECE Department, Carnegie Mellon University, Pittsburgh PA, USA*
Guest lecture on “Advanced Topics in Interconnection Networks" for the graduate-level **18-740/15-740 Computer Architecture** course (http://www.ece.cmu.edu/~ece740), November 1, 2013

Spring 2011 *ECE Department, Carnegie Mellon University, Pittsburgh PA, USA*
Delivered two guest lectures on "Advanced and Research Topics in Interconnection Networks" for the graduate-level **18-742 Parallel Computer Architecture** course (http://www.ece.cmu.edu/~ece742), February, 2011

Spring 2009 *ECE Department, Carnegie Mellon University, Pittsburgh PA, USA*
Guest lecture on "Virtual Memory" for the graduate-level **18-741 Advanced Computer Architecture** course (http://www.ece.cmu.edu/~ece741), February, 2009

Teaching Assistant

Spring 2011 *Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*
15-418 : Parallel Computer Architecture & Programming (http://www.cs.cmu.edu/~15418)

Spring 2009 *Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*
18-741 : Advanced Computer Architecture (http://www.ece.cmu.edu/~ece741)

Spring 2007 *Computer Science Department, University of Crete, Heraklion Crete, Greece*
CS-225 : Computer Organization (http://www.csd.uoc.gr/~hy225)

Fall 2006 *Computer Science Department, University of Crete, Heraklion Crete, Greece*
CS-220 : Digital Circuits Lab (http://www.csd.uoc.gr/~hy220)

Spring 2006 *Computer Science Department, University of Crete, Heraklion Crete, Greece*
CS-325 : Embedded Processors and Systems (http://www.csd.uoc.gr/~hy325)

Fall 2005 *Computer Science Department, University of Crete, Heraklion Crete, Greece*
CS-120 : Digital Design (http://www.csd.uoc.gr/~hy120)

Student Mentor

Summer 2014 Mentored undergraduate ECE student Raghav Gupta, who experimented with the PyEvolve genetic algorithms framework.

Fall 2012 Mentored undergraduate ECE student Taylor Womack, who worked on FPGA-based Network-on-Chip modeling.

Fellowships & Awards

Carnegie Mellon University *Graduate Fellowship, Computer Science Department, Carnegie Mellon University,*
2007-Present *Pittsburgh PA, USA* (http://www.cs.cmu.edu)

Intel *Intel PhD Fellowship, Intel Corporation* (https://www.intelfellowships.com)
2012-2013 Awarded to exceptional PhD candidates pursuing leading-edge innovation in fields related to Intel's business and research interests. Selected students are recognized as being amongst the best in their areas of research.

Carnegie Mellon University *Best Student Presentation Award, Computer Architecture Lab at Carnegie Mellon,*
2012 *Carnegie Mellon University, Pittsburgh PA, USA* (http://www.ece.cmu.edu/calcm)

MEMOCODE *2011*
*Awarded first place in the 2011 Memocode Hardware/Software Codesign contest on accelerating Network-on-Chip simulations (*http://bit.ly/memocode2011designcontest). My FPGA-accelerated design achieved the highest performance out of all contest entries.

IEEE Micro Top Picks *2010*
Top Picks in Computer Architecture, IEEE Micro, 2010 (www.computer.org/micro) Awarded to each year's most significant research publications in Computer Architecture based on novelty and industry relevance.

ICS, FORTH *2005,2006,2007*
Graduate Fellowship, Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece (http://www.ics.forth.gr/carv)

State Scholarships Foundation *2004*
Greek State Scholarship for academic excellence, Greek State Scholarships Foundation (http://www.iky.gr)
Awarded to select top-ranked students in various departments across the country.

ICS, FORTH *2004*
Undergraduate Fellowship, Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece (http://www.ics.forth.gr/carv)

IACM, FORTH *2001, 2002, 2003*
Undergraduate Fellowship, Institute of Applied and Computational Mathematics (IACM), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece (http://www.iacm.forth.gr)

Greek Ministry of Education *2001*
Award for Best Academic Performance
Graduated first in class with GPA 18.8 (out of 20)

Greek Ministry of Education *1996, 1997, 1998, 1999, 2000, 2001*
Award of Excellence for Academic Performance
Awarded to highest ranked students maintaining an "excellent" GPA (>18.5 out of 20).

Publications

DAC *2015*
Michael K. Papamichael, Peter Milder and James C. Hoe. **"Nautilus: Fast Automated IP Design Space Search Using Guided Genetic Algorithms"**, To appear in the *2015 Design Automation Conference (DAC)*, San Francisco, CA, June 7-11, 2015

ISPASS *2015*
Michael K. Papamichael, Cagla Cakir, Chen Sun, Chia-Hsin Owen Chen, James C. Hoe, Ken Mai, Li-Shiuan Peh and Vladimir Stojanovic. **"DELPHI: A Framework for RTL-Based Architecture Design Evaluation Using DSENT Models"**, To appear in the *2015 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Philadelphia, PA, March 29-31, 2015

FCCM *2013*
Eric S. Chung and Michael K. Papamichael. **"ShrinkWrap: Compiler-Enabled Optimization and Customization of Soft Memory Interconnects"**, *21st IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Seattle, WA, April 28-30, 2013

FPGA *2012*
Michael K. Papamichael and James C. Hoe. **"CONNECT: Re-Examining Conventional Wisdom for Designing NoCs in the Context of FPGAs"**, *20th ACM/ SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 22-24, 2012

FPGA *2012* Eric Chung, Michael K. Papamichael, Gabriel Weisz, James Hoe and Ken Mai. **"The Feasibility and Effectiveness of the CoRAM Memory Architecture for FPGA-Based Computing"**, *20th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 22-24, 2012

MEMOCODE *2011* Michael K. Papamichael. **"Fast Scalable FPGA-Based Network-on-Chip Simulation Models"**, *9th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Cambridge, UK, July 11-13, 2011

NOCS *2011* Michael K. Papamichael, James C. Hoe, and Onur Mutlu. **"FIST: A Fast, Lightweight, FPGA-Friendly Packet Latency Estimator for NoC Modeling in Full-System Simulations"**, *5th ACM/IEEE International Symposium on Networks-on-Chip (NOCS)*, Pittsburgh, PA, May 1-4, 2011

IEEE MICRO TOP PICKS *2011* Yoongu Kim, Michael Papamichael, Onur Mutlu and Mor Harchol-Balter. **"Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior"**, *IEEE Micro, Special Issue: Micro's Top Picks from 2010 Computer Architecture Conferences*

MICRO *2010* Yoongu Kim, Michael Papamichael, Onur Mutlu and Mor Harchol-Balter. **"Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior"**, *International Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, Dec 4-8, 2010

ACM TRETS *2009* Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi and Ken Mai, **"ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs"**, *ACM Transactions on Reconfigurable Technology and Systems*, 2009

WARP *2008* Eric S. Chung, Michael Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi and Ken Mai, **"An MP Architectural Exploration Vehicle using FPGA-accelerated Simulation"**, *3rd Workshop on Architectural Research Prototyping*, Beijing, China, June 21-22, 2008

FORTH *2007* Michael K. Papamichael. **"Network Interface Architecture and Prototyping for Chip and Cluster Multiprocessors"**, *FORTH-ICS Technical Report, TR392-07-2007*, July 2007

SAMOS VII *2007* V. Papaefstathiou, D. Pnevmatikatos, M. Marazakis, G. Kalokairinos, A. Ioannou, M. Papamichael, S. Kavadias, G. Mihelogiannakis and M. Katevenis. **"Prototyping Efficient Interprocessor Communication Mechanisms"**, *7th International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 16-19, 2007

HiPEAC *2006* V. Papaefstathiou, G. Kalokairinos, A. Ioannou, M. Papamichael, G. Mihelogiannakis, S. Kavadias, E. Vlachos, D. Pnevmatikatos and M. Katevenis. **"An FPGA-based Prototyping Platform for Research in High-Speed Interprocessor Communication"**, *2nd Industrial Workshop of the European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC)*, Eindhoven, Netherlands, October 17, 2006

FORTH *2006* *G. Kalokairinos, V. Papaefstathiou, A. Ioannou, D. Simos, M. Papamichael, G. Mihelogiannakis, M. Marazakis, D. Pnevmatikatos, and M. Katevenis.* **"Design and Implementation of a Multi-Gigabit NIC and a Scalable Buffered Crossbar Switch"**, *FORTH-ICS Technical Report, TR376-04-2006*, April 2006

Manuscripts Under Review

IEEE Computer *2015* Michael K. Papamichael and James C. Hoe. **"The CONNECT Network-on-Chip IP Generator"**, *IEEE Computer*

Talks & Tutorials

Stanford *2013* Michael K. Papamichael and James C. Hoe. **"CONNECT: Re-Examining Conventional Wisdom for Designing NoCs in the Context of FPGAs"**, Invited talk while visiting Stanford's VLSI Research Group, Palo Alto, CA, USA, February 13, 2013.

FPGA *2013* Michael K. Papamichael. Presented part of tutorial on using **"The CONNECT Network-on-Chip Generator"**, FPGA 2013, Monterey, CA, USA, February 11, 2013

MICRO *2012* Eric S. Chung and Michael K. Papamichael. Co-presented tutorial on **"Cross-Platform FPGA Accelerator Development Using the CoRAM Virtual Architecture and the CONNECT Network-on-Chip Generator"**, MICRO-45, Vancouver, Canada, December 2, 2012

Intel Labs *2012* Michael K. Papamichael and James C. Hoe. **"CONNECT: Fast Flexible FPGA-Tuned Networks-on-Chip",** *Invited talk while attending the 2012 Intel PhD Fellowship Forum, Intel Labs, Portland, OR, USA, June 2012*

CARL *2012* Michael K. Papamichael and James C. Hoe, **"CONNECT: Fast Flexible FPGA-Tuned Networks-on-Chip",** 2nd Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL 2012), Portland, OR, June 10, 2012.

FPGA *2012* Michael K. Papamichael and James C. Hoe. **"CONNECT: Re-Examining Conventional Wisdom for Designing NoCs in the Context of FPGAs"**, To appear in 20th ACM/ SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2012), Monterey, CA, February 23, 2012.

MEMOCODE *2011* Michael K. Papamichael. **"Fast Scalable FPGA-Based Network-on-Chip Simulation Models",** Invited talk as the winner of the first prize in the Absolute Performance Category of the annual *Memocode Hardware/Software Codesign contest*, 9th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2011), Cambridge, UK, July 11, 2011.

NOCS *2011* Michael K. Papamichael, James C. Hoe and Onur Mutlu. **"FIST: A Fast, Lightweight, FPGA-Friendly Packet Latency Estimator for NoC Modeling in Full-System Simulations"**, 5th ACM/IEEE International Symposium on Networks on Chip, Pittsburgh, PA, USA, May 3, 2011

ISPASS *2010* Eric S. Chung and Michael K. Papamichael. Co-presented tutorial **"RAMP Simulator Tutorial: Protoflex, FAST, HAsim, and RAMP-Gold"**, *ISPASS-2010, White Plains, NY, USA, March 28-30, 2010*

RAMP Retreat *2010* Michael K. Papamichael, Eric Chung, James C. Hoe, Babak Falsafi and Ken Mai, **"FIST: Fast Interconnect Simulation Techniques"**, *RAMP Retreat, Santa Cruz, CA, USA,* January 29, 2010

MICRO *2009* Eric S. Chung, Michael K. Papamichael and Mike Ferdman. Co-presented tutorial **"SimFlex and ProtoFlex: Fast, Accurate, and Flexible Simulation of Computer Systems"**, *MICRO-42, New York, NY, USA, December 12-16, 2009*

RAMP Retreat *2009* Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi and Ken Mai, **"The Open Source ProtoFlex Simulator"**, *RAMP Retreat, Austin, TX, USA,* June 25, 2009

IISWC *2009* Eric S. Chung and Michael K. Papamichael. Co-presented tutorial **"ProtoFlex: An Architectural Exploration Vehicle using FPGA-Accelerated, Full-System Multiprocessor Simulation"**, *IISWC-2009, Austin, TX, USA, October 4-6, 2009*

SUN Microsystems *2008* Michael K. Papamichael, Eric S. Chung, James C. Hoe, Babak Falsafi and Ken Mai, **"ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation"**, *SUN Microsystems Annual Internal Verification Summit, Santa Clara, CA, USA,* October 29, 2008

RAMP Retreat *2008* Michael K. Papamichael, Eric S. Chung, James C. Hoe, Babak Falsafi and Ken Mai, **"ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation"**, *RAMP Retreat, Stanford University, Palo Alto, CA, USA,* August 19, 2008

ASPLOS *2008* Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi and Ken Mai, Co-presented tutorial **"ProtoFlex Tutorial: Full-System MP Simulations Using FPGAs"**, *ASPLOS XIII Tutorial, Seattle, WA, USA, March 2, 2008*

SUN Microsystems *2008* Michael K. Papamichael**,** Wei Yu, Yongjun Jeon, Eric Chung and James C. Hoe. **"FACS: FPGA-Accelerated Multiprocessor Cache Simulator"**, *SUN Microsystems, Santa Clara, CA, USA,* January 18, 2008

University of Crete *2007* Michael K. Papamichael, **"Network Interface Architecture and Prototyping for Chip and Cluster Multiprocessors"**, *Master Thesis Defense, University of Crete, Greece,* July 10, 2007

Posters

FPGA *2013* Eric S. Chung and Michael K. Papamichael. **"Towards Automatic Customization of Interconnect and Memory in the CoRAM Abstraction"**, 21st ACM/ SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2013), Monterey, CA, February, 2013

Intel *2012* Michael K. Papamichael and James C. Hoe. **"CONNECT: Fast Flexible FPGA-Tuned Networks-on-Chip"**, 2012 Intel PhD Fellowship Forum, Hillsboro, OR, August 19-21, 2012

NOCS *2011* Michael K. Papamichael, James C. Hoe and Onur Mutlu. **"FIST: A Fast, Lightweight, FPGA-Friendly Packet Latency Estimator for NoC Modeling in Full-System Simulations"**, 5th ACM/IEEE International Symposium on Networks on Chip, Pittsburgh, PA, May 3, 2011

RAMP Retreat *2010* Eric S. Chung**,** Michael K. Papamichael, James C. Hoe, Babak Falsafi and Ken Mai. **"The Open-Source ProtoFlex Simulator"**, RAMP Retreat, Santa Cruz, CA, USA, January 29, 2010

C2S2 *2009* Eric S. Chung**,** Michael K. Papamichael**,** James C. Hoe, Babak Falsafi and Ken Mai. **"ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs"**, Center for Circuit and System Solutions (C2S2) Annual Review, IBM T.J. Watson Laboratory, Yorktown Heights, NY, April, 2009

RAMP Retreat *2008* Michael K. Papamichael**,** Eric S. Chung, James C. Hoe, Babak Falsafi and Ken Mai. **"Protoflex: Complexity-Effective FPGA-Accelerated Instrumentation"**, RAMP Retreat, Stanford University, Palo Alto, CA, USA, August 19, 2008

ASPLOS *2008* Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi and Ken Mai. **"An MP Architectural Exploration Vehicle Using Complexity-Effective FPGA-Accelerated Simulation"**, ASPLOS XIII, Seattle, WA, USA, March 2, 2008

RAMP Retreat *2008* Michael K. Papamichael, Wei Yu and Yongjun Jeon. **"Protoflex: Complexity-Effective FPGA-Accelerated Instrumentation"**, RAMP Retreat, University of California, Berkeley, CA, USA, January 16, 2008

ACACES *2007* V. Papaefstathiou and **M. Papamichael** (in collaboration with S. Kavadias, G. Kalokairinos, D. Pnevmatikatos and M. Katevenis). **"Interprocessor Communication: Towards Cache Integrated Network Interfaces"**, Poster presented at the 3rd HiPEAC Advanced Computer Architecture and Compilation for Embedded Systems (ACACES 2007), L' Aquila, Italy, 15-20 July 2007

OCIN *2006* V. Papaefstathiou, G. Kalokairinos, A. Ioannou, M. Papamichael, G. Mihelogiannakis, S. Kavadias, E. Vlahos, D. Pnevmatikatos and M. Katevenis. **"An FPGA-based Prototyping Platform for Research in High-Speed Interprocessor Communication"**, Poster presented at the 2006 Workshop on On- and Off-Chip Interconnection Networks for Multicore Systems (OCIN2006), 6-7 December 2006, Stanford, CA, USA.

Professional Activities

External Reviewer

MICRO *2014* 47th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Cambridge, UK, December 2014

NOCS *2014* 8th International Symposium on Networks-on-Chip (NOCS), Ferrara, Italy, September 2014

HPCA *2014* 20th International Symposium on High-Performance Architecture (HPCA), Orlando, FL, February 2014

MICRO *2014* 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Davis, CA, December 2013

NOCS *2013* 7th International Symposium on Networks-on-Chip (NOCS), Tempe, AZ, April 2013

FPGA *2013* 21st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), Monterey, CA, February 2013

CASES *2012* International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES), Tampere, Finland, October 2012

MICRO *2012* 45th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Vancouver, Canada, December 2012

HPCA *2012* 18th International Symposium on High-Performance Architecture (HPCA), New Orleans, Louisiana, February 2012

CASES *2011* International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES), Taipei, Taiwan, October 2011

ACM TRETS *2011* ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2011

HPCA *2011* 17th International Symposium on High-Performance Architecture (HPCA), San Antonio, TX, February 2011

ISPASS *2010* 2010 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), White Plains, NY, March 2010

HPCA *2010* 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Bangalore, India, January 2010

Departmental Activities

Doctoral Review Committee *2013-Present* Serving on the Computer Science Department Doctoral Review Committee (DRC), which is the official advisory committee to the Graduate Programs Administrator of the PhD Program and the Department Head.

CSD Ombudsperson *2013-Present* Serving as the Carnegie Mellon Computer Science Department Ombudsperson (http://www.csd.cs.cmu.edu/education/phd/omb.html).

Speakers Club *2010-Present* Serving as a member of the Computer Science Department "Speakers Club" (http://webapps.cs.cmu.edu/speakersclub/).

Technical Skills

Hardware Development Tools Extensive experience with Bluespec System Verilog, Verilog-XL, Modelsim, Cadence NCLaunch, Synopsys VCS, Synopsys Design Compiler, Synopsys TetraMAX, Synplify, Cadence Silicon Encounter, Xilinx ISE, Xilinx Vivado, Xilinx EDK, Xilinx Chipscope, Altera Max Plus II, Altera Quartus II, Eagle PCB Layout Editor, PCBExpress, Wickenhaeuser uC51

Basic knowledge of VHDL, Chisel, Hspice

Software Development Tools Fluent in C, C++, Java, Python, Ruby, PHP, SQL, MapBasic, Matlab, Bash, HTML

Basic knowledge of Fortran, Basic, Pascal, C#, Javascript, x86/SPARC assembly

System Administration Extensive experience with Linux administration. Set up and maintained (as the primary administrator) our research group's cluster of 50+ Linux machines, which among others, supported the Condor batch job management system, Andrew File System (AFS), Network File System (NFS), Kerberos, automated system management and monitoring through custom-developed maintenance scripts, Puppet and Nagios, as well as multiple SW and HW development tools and environments (e.g., Synopsys Design Compiler, Cadence SoC Encounter, Modelsim, Xilinx ISE/Vivado/EDK).

Extracurricular Activities

Squash, racquetball, tennis, table tennis, volleyball, snowboarding, building and flying custom-designed radio controlled airplanes.