

---

**Personal**

*Date of Birth:* July 5, 1983  
*Citizenship:* United States of America  
*Languages:* Fluent in English, Greek and German



---

**Contact Information**

*Address:* 5000 Forbes Ave  
Pittsburgh, PA 15213  
U.S.A.

*Phone:* +1 (412) 268-9611  
*Cell:* +1 (412) 973-2662  
*E-mail:* [papamix@cs.cmu.edu](mailto:papamix@cs.cmu.edu) or [papamix@gmail.com](mailto:papamix@gmail.com)  
*Homepage:* <http://www.cs.cmu.edu/~mpapamic>

---

**Education**

**PhD** *Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*  
*September 2007 - Present* (<http://www.cs.cmu.edu>)

*Research Area:* Networks-on-Chip, CMP & reconfigurable architectures, FPGA-accelerated simulation

*GPA:* 4.0/4.0

*Advisor:* Prof. James C. Hoe (<http://www.ece.cmu.edu/~jho>)

*Graduate Courses Taken:* 15-781: Machine Learning  
15-750: Graduate Algorithms  
15-740: Advanced Computer Architecture  
15-744: Graduate Computer Networks  
15-814: Type Systems and Programming Languages  
18-742: Parallel Computer Architecture  
18-760: VLSI CAD: Logic to Layout  
18-760: Advanced Digital IC Design

**Master of Science** *Computer Science Department, University of Crete, Heraklion Crete, Greece*  
*July 2007* (<http://www.csd.uoc.gr>)

*Major:* Architecture of Microelectronic Systems

*Minor:* Parallel and Distributed Systems

*Thesis Title:* Network Interface Architecture and Prototyping for Chip and Cluster Multiprocessors

*GPA:* 9.78 out of 10 – ranked first among all graduate students of the department

*Major Professor:* Prof. Manolis Katevenis (<http://www.ics.forth.gr/~kateveni>)

*Graduate Courses Taken:* CS-422: VLSI Systems (<http://www.csd.uoc.gr/~hy422>)  
CS-425: Computer Systems Architecture (<http://www.csd.uoc.gr/~hy425>)  
CS-527: Parallel Computer Architecture (<http://www.csd.uoc.gr/~hy527>)  
CS-534: Packet Switch Architecture (<http://www.csd.uoc.gr/~hy534>)  
CS-527: Parallel Systems and Grids (<http://www.csd.uoc.gr/~hy527>)  
CS-556: Distributed Systems (<http://www.csd.uoc.gr/~hy556>)  
CS-558: Internet Technologies and Systems (<http://www.csd.uoc.gr/~hy558>)  
CS-523: EDA Tools for Digital VLSI Systems (<http://www.csd.uoc.gr/~hy523>)  
CS-590.24: Algorithms of CAD Tools (<http://www.csd.uoc.gr/~hy590-24>)

**ACACES** *Second and Third International Summer School on Advanced Computer Architecture and*  
*2006,2007* *Compilation for Embedded Systems (ACACES), European Network of Excellence on High-*  
*Performance Embedded Architecture and Compilation (HiPEAC), July 23 – 29 2006,*  
*L'Aquila, Italy (<http://www.hipeac.net/acaces2006/>) and July 15 – 20 2007, L'Aquila, Italy*  
*(<http://www.hipeac.net/acaces2007/>)*

The International ACACES Summer School is a one week summer school for computer architects and compiler builders working in the field of high performance computer architecture and compilation for embedded systems.

*Courses 2006* Multicore & Multiprocessor Interconnection Networks (Prof. Timothy Pinkston)  
Thread-Level Parallelism and Transactional Memory (Prof. Mark Hill)  
Compiling for Embedded Design Constraints (Prof. David Whalley)  
Compiler Optimizations Research in GCC (Dr. Albert Cohen)

*Courses 2007* Coherence, Store Atomicity, and Memory Consistency Models (Prof. Michael Dubois)  
Chip Multiprocessor (CMP) Architectures (Prof. Kunle Olukotun)  
Parallel Programming Models (Prof. Lawrence Rauchwerger)  
Queue and Flow Control Architectures for Interconnection Switches (Prof. M. Katevenis)

**Computer Science Diploma** *Computer Science Department, University of Crete, Heraklion Crete, Greece*  
*2005* (<http://www.csd.uoc.gr>)

Four-year professional degree program, equivalent to Bachelor of Science in Computer Science.

*Diploma Thesis Title:* SRAM Multiple Access Controller & Related Subsystems for a High-speed Network Interface Card

*GPA:* 8.78 out of 10 (excellent)

**Abitur Diploma** *German School of Thessaloniki, Thessaloniki, Greece* (<http://www.dst.gr>)  
*2001*

German school graduation certificate for university entrance issued after final exams in German language and two specialization subjects. (<http://en.wikipedia.org/wiki/Abitur>)

*Specialization Subjects:* Mathematics and Physics

*GPA:* 1.2 (scale is 1.0 to 6.0, with 1.0 being the highest possible grade)

**High School Diploma** *German School of Thessaloniki, Thessaloniki, Greece* (<http://www.dst.gr>)  
*2001*

*GPA:* 18.8 out of 20 (graduated first in class)

---

## Technical Skills

**Hardware Development Tools** Extensive experience with Bluespec System Verilog, Verilog-XL, Modelsim, Cadence NCLaunch, Synopsys VCS, Synopsys Design Compiler, Synopsys TetraMAX, Synplify, Cadence Silicon Encounter, Xilinx ISE, Xilinx EDK, Xilinx Chipscope, Altera Max Plus II, Altera Quartus II, Eagle PCB Layout Editor, PCBExpress, Wickenhaeuser uC51

Basic knowledge of VHDL, Hspice.

**Software Development Tools** Fluent in C, C++, Java, Python, Ruby, PHP, SQL, MapBasic, Matlab, HTML

Basic knowledge of Fortran, Basic, Pascal, C#, Awk, Javascript, x86/SPARC assembly

---

## Research Experience

**PhD Candidate** *Computer Architecture Lab at Carnegie Mellon (CALCM), Carnegie Mellon University, Pittsburgh PA, USA (<http://www.ece.cmu.edu/calcm>)*  
2007-Present

2011-Present **CONNECT:** As the lead student in this project I proposed a new Network-on-Chip (NoC) architecture specifically tailored for FPGA implementation. To support this research, I developed CONNECT, an NoC generator that can produce synthesizable RTL designs of FPGA-tuned multi-node NoCs of arbitrary topology. The CONNECT NoC architecture embodies a set of FPGA-motivated design principles that uniquely influence key NoC design decisions, such as topology, link width, router pipeline depth, network buffer sizing, and flow control and in many cases go against conventional wisdom stemming from traditional ASIC-oriented NoC designs. CONNECT is used as the main interconnection network within the CoRAM project (<http://www.ece.cmu.edu/~coram>), our research group's effort to explore a novel architecture for future FPGAs.

2010-2011 **FIST:** As the lead student in this project I developed a set of fast, lightweight, FPGA-friendly NoC models that closely capture the behavior of time-consuming detailed NoC models in full-system performance simulators.

2010 **Thread Cluster Memory (TCM) Scheduling:** In this project I co-developed a new memory scheduler that exploits differences in the memory behavior of threads to maximize system throughput and fairness (TCM, an IEEE Micro 2010 Top Picks)

2007-2009 **ProtoFlex:** For the purposes of the ProtoFlex project (<http://www.ece.cmu.edu/~protoflex>) I designed and implemented FPGA-accelerated instrumentation components to achieve faster full-system high-fidelity computer architecture simulations. Instrumentation examples:

- Functional model of Piranha-like functional CMP cache hierarchy (in Verilog)
- Model of 2-level CMP Branch Predictor (in Bluespec System Verilog)

**Research Intern at Intel Labs** *Microarchitecture Research Lab (MRL), Intel Labs, Santa Clara, CA, USA*  
July 2010- October 2010 (<http://techresearch.intel.com>)

Worked on uncore modeling for emerging multiprocessor systems.

*Mentor:* Dr. Graham Schelle  
*Supervisor:* Dr. Hong Wang (<http://techresearch.intel.com/ResearcherDetails.aspx?Id=214>)

**Graduate Student Research Assistant** *Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece*  
2005-2007 (<http://www.ics.forth.gr/carv>)

Design and implementation of a network interface with multiple queue support for use in the FPGA-based prototyping platform of the CARV laboratory for the purposes of the SARC project. (<http://www.sarc-ip.org>)

*Supervisor:* Prof. Manolis Katevenis (<http://www.ics.forth.gr/~kateveni>)

**Student Research Assistant** *Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece*  
2004-2005 (<http://www.ics.forth.gr/carv>)

Design and implementation of an SRAM multiple access controller and other related subsystems for use in the high-speed network interface card in the FPGA-based prototyping platform of the CARV laboratory for the purposes of the cross-European project SIVSS. (<http://www.sivss.org>).

*Supervisor:* Prof. Manolis Katevenis (<http://www.ics.forth.gr/~kateveni>)

**Student Research Assistant** *Institute of Applied and Computational Mathematics (IACM), Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece*  
2001-2004 (<http://www.iacm.forth.gr>)

Lead Software Developer in the “OASA” project for the Extension of the GIS system of the Athens Urban Transport Organization.  
(<http://www.iacm.forth.gr/regional/projects/auto-gis.html>)

Manipulation and enrichment of vector maps with GIS data for the company Infocharta.  
(<http://www.infocharta.gr/>)

*Supervisor:* Dr. Poulicos Prastakos (<http://www.iacm.forth.gr/regional/people/prastakos.html>)

---

## Teaching Experience

**Teaching Assistant** *Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*  
Spring 2011 **15-418 : Parallel Computer Architecture & Programming**  
(<http://www.cs.cmu.edu/~15418>)

**Teaching Assistant** *Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*  
Spring 2009 **18-741 : Advanced Computer Architecture** (<http://www.ece.cmu.edu/~ece741>)

- Teaching Assistant** *Computer Science Department, University of Crete, Heraklion Crete, Greece*  
*Spring 2007* **CS-225 : Computer Organization** (<http://www.csd.uoc.gr/~hy225>)
- Teaching Assistant** *Computer Science Department, University of Crete, Heraklion Crete, Greece*  
*Fall 2006* **CS-220 : Digital Circuits Lab** (<http://www.csd.uoc.gr/~hy220>)
- Teaching Assistant** *Computer Science Department, University of Crete, Heraklion Crete, Greece*  
*Spring 2006* **CS-325 : Embedded Processors and Systems** (<http://www.csd.uoc.gr/~hy325>)
- Teaching Assistant** *Computer Science Department, University of Crete, Heraklion Crete, Greece*  
*Fall 2005* **CS-120 : Digital Design** (<http://www.csd.uoc.gr/~hy120>)
- 

## Fellowships & Awards

- Carnegie Mellon University** *Graduate Fellowship, Computer Science Department, Carnegie Mellon University, Pittsburgh PA, USA*  
*2007-Present* (<http://www.cs.cmu.edu>)
- MEMOCODE** *Awarded first place in the Absolute Performance category of the 2011 Memocode Hardware/Software Codesign contest*  
*2011* (<http://bit.ly/memocode2011designcontest>)
- IEEE Micro Top Picks** *Top Picks in Computer Architecture, IEEE Micro, 2010* ([www.computer.org/micro](http://www.computer.org/micro))  
*2010* awarded to each year's most significant research publications in Computer Architecture based on novelty and industry relevance.
- ICS, FORTH** *Graduate Fellowship, Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece*  
*2005,2006,2007* (<http://www.ics.forth.gr/carv>)
- State Scholarships Foundation** *Greek State Scholarship for academic excellence, Greek State Scholarships Foundation*  
*2004* (<http://www.iky.gr>)
- ICS, FORTH** *Undergraduate Fellowship, Computer Architecture and VLSI Systems (CARV) laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece*  
*2004* (<http://www.ics.forth.gr/carv>)
- IACM, FORTH** *Undergraduate Fellowship, Institute of Applied and Computational Mathematics (IACM), Foundation for Research and Technology Hellas (FORTH), Heraklion, Crete, Greece*  
*2001, 2002, 2003* (<http://www.iacm.forth.gr>)
- Greek Ministry of Education** *Award for Best Academic Performance*  
*2001* graduated first in class with GPA 18.8 (out of 20)
- Greek Ministry of Education** *Award of Excellence for Academic Performance*  
*1996, 1997, 1998, 1999, 2000, 2001*
- 

## Publications

- FPGA** Michael K. Papamichael and James C. Hoe. "**CONNECT: Re-Examining Conventional Wisdom for Designing NoCs in the Context of FPGAs**", To appear in 20th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2012), Monterey, CA, February 22-24, 2012.

- FPGA** 2012 Eric Chung, Michael Papamichael, Gabriel Weisz, James Hoe and Ken Mai. "**The Feasibility and Effectiveness of the CoRAM Memory Architecture for FPGA-Based Computing**", To appear in 20th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2012), Monterey, CA, February 22-24, 2012.
- MEMOCODE** 2011 Michael K. Papamichael. "**Fast Scalable FPGA-Based Network-on-Chip Simulation Models**", 9th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2011), Cambridge, UK, July 11-13, 2011.
- NOCS** 2011 Michael K. Papamichael, James C. Hoe, and Onur Mutlu. "**FIST: A Fast, Lightweight, FPGA-Friendly Packet Latency Estimator for NoC Modeling in Full-System Simulations**", 5th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2011), Pittsburgh, PA, May 1-4, 2011.
- IEEE MICRO TOP PICKS** 2011 Yoongu Kim, Michael Papamichael, Onur Mutlu, Mor Harchol-Balter. "**Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior**", IEEE Micro, Special Issue: Micro's Top Picks from 2010 Computer Architecture Conferences
- IEEE MICRO** 2010 Yoongu Kim, Michael Papamichael, Onur Mutlu, Mor Harchol-Balter. "**Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior**", International Symposium on Microarchitecture (MICRO-43), Atlanta, GA, Dec 4-8, 2010
- ACM TRETs** 2009 Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi and Ken Mai, "**ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs**", *ACM Transactions on Reconfigurable Technology and Systems*, 2009
- WARP** 2008 Eric S. Chung, Michael Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai, "**An MP Architectural Exploration Vehicle using FPGA-accelerated Simulation**", *3rd Workshop on Architectural Research Prototyping, Beijing, China, June 21-22, 2008*
- FORTH** 2007 Michael K. Papamichael. "**Network Interface Architecture and Prototyping for Chip and Cluster Multiprocessors**", FORTH-ICS Technical Report, TR392-07-2007, July 2007
- SAMOS VII** 2007 V. Papaefstathiou, D. Pnevmatikatos, M. Marazakis, G. Kalokairinos, A. Ioannou, M. Papamichael, S. Kavadias, G. Mihelogiannakis and M. Katevenis. "**Prototyping Efficient Interprocessor Communication Mechanisms**", Accepted for presentation at the 7<sup>th</sup> International Symposium on Systems, Architectures, MOdeling and Simulation (SAMOS), Samos, Greece, July 16-19, 2007
- HiPEAC** 2006 V. Papaefstathiou, G. Kalokairinos, A. Ioannou, M. Papamichael, G. Mihelogiannakis, S. Kavadias, E. Vlachos, D. Pnevmatikatos and M. Katevenis. "**An FPGA-based Prototyping Platform for Research in High-Speed Interprocessor Communication**", 2nd Industrial Workshop of the European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC), Eindhoven, Netherlands, October 17, 2006
- FORTH** 2006 G. Kalokairinos, V. Papaefstathiou, A. Ioannou, D. Simos, M. Papamichael, G. Mihelogiannakis, M. Marazakis, D. Pnevmatikatos, and M. Katevenis. "**Design and Implementation of a Multi-Gigabit NIC and a Scalable Buffered Crossbar Switch**", FORTH-ICS Technical Report, TR376-04-2006, April 2006

---

**Talks & Tutorials**

- MEMOCODE 2011** Michael K. Papamichael. "Fast Scalable FPGA-Based Network-on-Chip Simulation Models", 9th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2011), Cambridge, UK, July 11, 2011.
- NOCS 2011** Michael K. Papamichael, James C. Hoe and Onur Mutlu. "FIST: A Fast, Lightweight, FPGA-Friendly Packet Latency Estimator for NoC Modeling in Full-System Simulations", 5th ACM/IEEE International Symposium on Networks on Chip, Pittsburgh, PA, USA, May 3, 2011
- ISPASS 2010** Eric S. Chung, Michael K. Papamichael. "*RAMP Simulator Tutorial: Protoflex, FAST, HAsim, and RAMP-Gold*", ISPASS-2010, White Plains, NY, USA, March 28-30, 2010
- RAMP Retreat 2010** Michael K. Papamichael, Eric Chung, James C. Hoe, Babak Falsafi and Ken Mai, "*FIST: Fast Interconnect Simulation Techniques*", RAMP Retreat, Santa Cruz, CA, USA, January 29, 2010
- MICRO 2009** Eric S. Chung, Michael K. Papamichael, Mike Ferdman. "*SimFlex and ProtoFlex: Fast, Accurate, and Flexible Simulation of Computer Systems*", MICRO-42, New York, NY, USA, December 12-16, 2009
- RAMP Retreat 2009** Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi and Ken Mai, "*The Open Source ProtoFlex Simulator*", RAMP Retreat, Austin, TX, USA, June 25, 2009
- IISWC 2009** Eric S. Chung, Michael K. Papamichael. "*ProtoFlex: An Architectural Exploration Vehicle using FPGA-Accelerated, Full-System Multiprocessor Simulation*", IISWC-2009, Austin, TX, USA, October 4-6, 2009
- SUN Microsystems 2008** Michael K. Papamichael, Eric S. Chung, James C. Hoe, Babak Falsafi and Ken Mai, "*ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation*", SUN Microsystems Annual Internal Verification Summit, Santa Clara, CA, USA, October 29, 2008
- RAMP Retreat 2008** Michael K. Papamichael, Eric S. Chung, James C. Hoe, Babak Falsafi and Ken Mai, "*ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation*", RAMP Retreat, Stanford University, Palo Alto, CA, USA, August 19, 2008
- ASPLOS 2008** Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi and Ken Mai, "*ProtoFlex Tutorial: Full-System MP Simulations Using FPGAs*", ASPLOS XIII Tutorial, Seattle, WA, USA, March 2, 2008
- SUN Microsystems 2008** Michael K. Papamichael, Wei Yu, Yongjun Jeon, Eric Chung, James C. Hoe. "*FACS: FPGA-Accelerated Multiprocessor Cache Simulator*", SUN Microsystems, Santa Clara, CA, USA, January 18, 2008
- University of Crete 2007** Michael K. Papamichael, "*Network Interface Architecture and Prototyping for Chip and Cluster Multiprocessors*", Master Thesis Defense, University of Crete, Greece, July 10, 2007

---

**Posters**

- NOCS 2011** **Michael K. Papamichael**, James C. Hoe and Onur Mutlu. "*FIST: A Fast, Lightweight, FPGA-Friendly Packet Latency Estimator for NoC Modeling in Full-System Simulations*", 5th ACM/IEEE International Symposium on Networks on Chip, Pittsburgh, PA, May 3, 2011
- RAMP Retreat 2010** **Eric S. Chung, Michael K. Papamichael**, , James C. Hoe, Babak Falsafi, Ken Mai. "*The Open-Source ProtoFlex Simulator*", RAMP Retreat, Santa Cruz, CA, USA, January 29, 2010
- RAMP Retreat 2008** **Michael K. Papamichael**, Eric S. Chung, James C. Hoe, Babak Falsafi, Ken Mai. "*Protoflex: Complexity-Effective FPGA-Accelerated Instrumentation*", RAMP Retreat, Stanford University, Palo Alto, CA, USA, August 19, 2008
- ASPLOS 2008** **Eric S. Chung, Michael K. Papamichael**, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "*An MP Architectural Exploration Vehicle Using Complexity-Effective FPGA-Accelerated Simulation*", ASPLOS XIII, Seattle, WA, USA, March 2, 2008
- RAMP Retreat 2008** **Michael K. Papamichael**, Wei Yu, Yongjun Jeon. "*Protoflex: Complexity-Effective FPGA-Accelerated Instrumentation*", RAMP Retreat, University of California, Berkeley, CA, USA, January 16, 2008
- ACACES 2007** V. Papaefstathiou and **M. Papamichael** (in collaboration with S. Kavadias, G. Kalokairinos, D. Pnevmatikatos and M. Katevenis). "*Interprocessor Communication: Towards Cache Integrated Network Interfaces*", Poster presented at the 3rd HiPEAC Advanced Computer Architecture and Compilation for Embedded Systems (ACACES 2007), L' Aquila, Italy, 15-20 July 2007
- OCIN 2006** V. Papaefstathiou, G. Kalokairinos, A. Ioannou, **M. Papamichael**, G. Mihelogiannakis, S. Kavadias, E. Vlahos, D. Pnevmatikatos and M. Katevenis. "*An FPGA-based Prototyping Platform for Research in High-Speed Interprocessor Communication*", Poster presented at the 2006 Workshop on On- and Off-Chip Interconnection Networks for Multicore Systems (OCIN2006), 6-7 December 2006, Stanford, CA, USA.

---

**Extracurricular Activities**

Squash, Racquetball, Tennis, Table tennis, Volleyball, Billiards, Snowboarding, Camping, Radio controlled airplanes and helicopters