Emulation of Multi-Hop Wireless Ad Hoc Networks

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1 Proof of the Reordering Algorithm

Notation:

- $e(n,t)$: event e happens at node n at time t.
- $e(E,t_1,t_2)$: the result of reordering operation (defined below) on $e(E,t)$, which means event e is scheduled at the emulated node E at time t_1, but dispatched at time t_2. The simulation clock is set to t_1 when this event is dispatched.
- $d(n,t)$: the distance between node n and its nearest neighbor at time t.
- $d(n_1,n_2,t)$: the distance between node n_1 and n_2 at time t.
- $Clock(n,t)$: the local simulation clock value of node n at the global simulation time t. For convenience, here we assume that there is a simulation clock associated with each node. When $e(n,t)$ or $e(n,t,t_2)$ is dispatched, $Clock(n,t)$ is set to t or t_2 respectively.
- C: the speed of light, which is $3 \times 10^8 m/s$
- V: the maximum speed of the mobile nodes during the whole simulation.

Reordering operation: An event $e(E,t)$ can be handled as $e(E,t,t')$, where

$$t' = \max\{t - d(E,t)/C + \frac{V}{C} * \frac{d(E,t)}{C},\ \ Clock(E,T)\}$$

Here T is the value of the global simulation clock when event $e(E,t)$ is being scheduled (or inserted into the event queue). In our implementation, $\frac{V}{C} * \frac{d(E,t)}{C}$ is neglected since it is so small compared to $\frac{d(E,t)}{C}$.

Claim: If we apply the *reordering operation* to all of the events belonging to emulated nodes, we still preserve the causality of the simulated model of multi-hop wireless ad hoc network.

Proof: Inside *ns-2*, a simulated/emulated node represents a physical node in the real world. Mobile nodes in *ns-2* exchange information by scheduling events in the global event queue, which is the only way for two mobile nodes to exchange messages in *ns-2*. Therefore the causality of the simulated model is preserved if the following local causality constraint is maintained: *each simulated node processes its events at non-decreasing time-stamp order.*

For any two events $e(E,t_1)$, $e(E,t_2)$ belonging to the same emulated node E, the reordering operation turns them into events of $e(E,t_1,t'_1)$ and $e(E,t_2,t'_2)$. Suppose $t_2 > t_1$, we need to show that $t'_2 > t'_1$. We have:

$$\begin{aligned}
|d(E,t_2) - d(E,t_1)| &\leq V*(t_2-t_1) \\
t'_2 &= \max\{t_2 - d(E,t_2)/C + \frac{V}{C} * \frac{d(E,t_2)}{C},\ \ Clock(E,T_2)\} \\
t'_1 &= \max\{t_1 - d(E,t_1)/C + \frac{V}{C} * \frac{d(E,t_1)}{C},\ \ Clock(E,T_1)\}
\end{aligned}$$

All we need to show is $t'_2 > t'_1$ for all possible values of t'_2 and t'_1.

- **case 1:**

$$\begin{aligned}
t'_2 &= t_2 - d(E,t_2)/C + \frac{V}{C} * \frac{d(E,t_2)}{C} \\
t'_1 &= t_1 - d(E,t_1)/C + \frac{V}{C} * \frac{d(E,t_1)}{C}
\end{aligned}$$

  If $d(E,t_2) < d(E,t_1)$, then it is obvious that $t'_2 > t'_1$ because $t_2 > t_1$. If $d(E,t_2) \geq d(E,t_1)$, we have: $t'_2 - t'_1 \geq (t_2 - t_1) * \left(1 - \frac{V}{C}(1 - V/C)\right) > 0$.[1]

- **case 2:**

$$\begin{aligned}
t'_2 &= Clock(E,T_2) \\
t'_1 &= t_1 - d(E,t_1)/C + \frac{V}{C} * \frac{d(E,t_2)}{C}
\end{aligned}$$

  Since $t'_2 = Clock(E,T_2) \geq t_2 - d(E,t_2)/V + \frac{V}{C} * \frac{d(E,t_2)}{C}$, from case 1 we have $t'_2 > t'_1$.

[1] because $V/C \ll 1$

- **case 3:**

$$
\begin{aligned}
t'_2 &= t_2 - d(E,t_2)/C + \frac{V}{C} * d(E,t_2)/C \\
t'_1 &= Clock(E,T_1)
\end{aligned}
$$

If $e(E,t_1)$ is already in the event queue when $e(E,t_2)$ is being inserted, then we must have $t'_2 > t'_1$ because $Clock(E,T_2) > Clock(E,T_1)$ [2]. So in the following proof for **case 3**, we only need to show $t'_2 > t'_1$ for the case that $e(E,t_2)$ is already in the event queue when $e(E,t_1)$ is being inserted into the queue.

We prove $t'_2 > t'_1$ by contradiction, that is, we assume $t'_1 \geq t'_2$. Based on this assumption, we will deduce that $t_1 \geq t_2$, which is in contradiction with our first assumption $t_1 < t_2$.

Suppose $t'_1 \geq t'_2$, we have $t'_1 = Clock(E,T_1) \geq t'_2$. Therefore, when $e(E,t_1)$ is generated, there must be at least one event belonging to node E which has been dispatched at time $t \geq t'_2$. So $e(E,t_1)$ must be the direct or indirect result of dispatching some event $e(n,t_y)$, with $t_y \geq t'_2$.

The event $e(n,t_y)$ can be one of the following two cases:

1. $e(n,t_y)$ doesn't belong to node E. The only way for a node n to schedule an event on another node E is to send a packet to E. Since $d(E,t_y)$ is the distance between node E and its nearest neighbor, we have $d(E,t_y) \leq d(n,E,t_y)$. Therefore:

$$
\begin{aligned}
t_1 &= t_y + d(n,E,t_y)/C \\
&\geq t'_2 + d(E,t_y)/C
\end{aligned} \tag{1}
$$

   If $d(E,t_y) > d(E,t_2)$, then $t_1 \geq t'_2 + d(E,t_2)/C > t_2$, which is in contradiction with the general assumption $t_1 < t_2$.

   If $d(E,t_y) \leq d(E,t_2)$, then

$$
\begin{aligned}
d(E,t_2) - d(E,t_y) &\leq V * (t_2 - t_y) \\
&< V * d(E,t_2)/C
\end{aligned} \tag{2}
$$

   Therefore, from (1) and (2), we have: $t_1 \geq t'_2 + (1 - V/C) * d(E,t_2)/C = t_2$, which is in contradiction with the general assumption $t_1 < t_2$.

[2] It is obvious that $t_2 > t_1 \Longrightarrow Clock(E,T_2) > Clock(E,T_1)$

2. $e(n, t_y)$ belongs to node E, that is, $n = E$. Due to the reordering operation, $e(n, t_y)$ is handled as $e(E, t_y, t_x)$, with $t_x > t'_2$. There are two possible ways to generate event $e(n, t_y)$:

   – $e(E, t_y)$ is scheduled by using NS command: *ns at time_ handler*. For this case, $Clock(E, T_x) = 0$.

   – $e(E, t_y)$ is the direct result of processing the event of $e(n_0, t_0)$, with $t_0 < t'_2$. When $e(n_0, t_0)$ is being processed, the local clock value of node E isn't greater than t'_2, because $e(E, t'_2)$ is not executed yet. Therefore, we have $t_x > t'_2 \geq Clock(E, T_x)$, or in other words, $t_x = t_y - d(E, t_y)/C + \frac{V}{C} * d(E, t_y)/C$.

   For both ways to generate $e(E, t_y)$, we have:

$$\begin{aligned} t_x &= t_y - d(E, t_y)/C + \frac{V}{C} * d(E, t_y)/C \\ t'_2 &= t_2 - d(E, t_2)/C + \frac{V}{C} * d(E, t_2)/C \end{aligned}$$

   According to the result of **case 1**, if $t_y < t_2$, then $t_x < t'_2$, which is in contradiction with $t_x > t'_2$. So there must be $t_2 \leq t_y$. Since $t_y \leq t_1$[3], we have $t_2 \leq t_1$, which is in contradiction with the general assumption $t_1 > t_2$.

- **case 4:**

$$\begin{aligned} t'_2 &= Clock(E, T_2) \\ t'_1 &= Clock(E, T_1) \end{aligned}$$

Since $t'_2 = Clock(E, T_2) \geq t_2 - d(E, t_2)/C + \frac{V}{C} * d(E, t_2)/C$, this case is reduced to **case 3**.

[3]because $e(n, t_y)$ generates $e(E, t_1)$