15-740/18-740 Computer Architecture

# Course Project Milestone Report

Athula Balachandran
Lavanya Subramanian

November 17, 2009

# 1 Major Changes

There are no major changes to the goal and the implementation that we stated during the project proposal.

# 2 What have we accomplished so far?

We are using the BLESS simulator for simulating the Chip Multiprocessor.

- We have built coarse grained power models into the simulator
- We have implemented thread motion support into the simulator and hence we are able to currently perform thread motion based on the frequency profiles of the processors and the application variability.

We have some initial results that show the performance degradation under different power budgets for a configuration with 2 different frequency/voltage levels for the processors. These are preliminary results can be found at our course project website

`http://www.cs.cmu.edu/~abalacha/15740/15740_milestone.html`

# 3 Meeting the milestone

We had set our milestone as implementing thread motion on the bless simulator and getting some preliminary results. And we have been successful in meeting this milestone.

# 4 Surprises

As far as the implementation is concerned, we did not have any major surprises since we were aware of the capabilities/limitations of the simulator from the start of the project. As a preliminary result, we expected to see that performing thread migration at fine grained intervals would lead to huge performance degradation. The preliminary results indicate this as well.

# 5 Revised Schedule

We need to now perform extensive simulation studies. In particular,

- We would also like to analyze the effect of migration interval on the power and performance degradation. This would be the key factor in determining the number of migrations and as a result, the performance degradation and power savings.
- We would like to study the performance under different numbers of frequency/voltage levels.

- The prediction mechanism that we currently use is a last value predictor, inspired by our main reference paper. We would also like to spend some time on trying to change the mechanism and see its effect on the performance degradation and power savings.

Finally our 125% goal is to model a shared L2 cache and fine tune the algorithm for minimizing L2 access latency. If time permits, we will work on the 125% goal that we set.

# 6 Resources Needed

The Bless simulator is our main resource. This simulator is a trace-based simulator and does not model instruction addresses or the L1 Instruction Cache. So, we do not account for the Instruction Cache going cold, following a migration. However, we model the effects due to the Data cache going cold and the loss of architectural state. These would constitute a major part of the performance degradation and as the preliminary results indicate, are representative.