Virtual Memory: Concepts

15-213: Introduction to Computer Systems
17th Lecture, July 5, 2018

Instructors:
Brian Railing
Hmmm, How Does This Work?!

Solution: Virtual Memory (today and next lecture)
Today

- Address spaces
- VM as a tool for caching
- VM as a tool for memory management
- VM as a tool for memory protection
- Address translation
A System Using Physical Addressing

- Used in “simple” systems like embedded microcontrollers in devices like cars, elevators, and digital picture frames
A System Using Virtual Addressing

- Used in all modern servers, laptops, and smart phones
- One of the great ideas in computer science
Address Spaces

- **Linear address space**: Ordered set of contiguous non-negative integer addresses:
  \{0, 1, 2, 3 \ldots \}

- **Virtual address space**: Set of \( N = 2^n \) virtual addresses
  \{0, 1, 2, 3, \ldots, N-1\}

- **Physical address space**: Set of \( M = 2^m \) physical addresses
  \{0, 1, 2, 3, \ldots, M-1\}
Why Virtual Memory (VM)?

- **Uses main memory efficiently**
  - Use DRAM as a cache for parts of a virtual address space

- **Simplifies memory management**
  - Each process gets the same uniform linear address space

- **Isolates address spaces**
  - One process can’t interfere with another’s memory
  - User program cannot access privileged kernel information and code
Today

- Address spaces
- **VM as a tool for caching**
- **VM as a tool for memory management**
- **VM as a tool for memory protection**
- Address translation
VM as a Tool for Caching

- Conceptually, *virtual memory* is an array of N contiguous bytes stored on disk.
- The contents of the array on disk are cached in *physical memory* (DRAM cache)
  - These cache blocks are called *pages* (size is $P = 2^p$ bytes)

![Diagram showing virtual memory and physical memory relationship]
Remember: Set Associative Cache

E = 2: Two lines per set
Assume: cache block size 8 bytes

Index to find set

Block offset

Address:

2 lines per set

S sets
DRAM Cache Organization

- DRAM cache organization driven by the enormous miss penalty
  - DRAM is about $10x$ slower than SRAM
  - Disk is about $10,000x$ slower than DRAM

- Consequences
  - Large page (block) size: typically 4 KB, sometimes 4 MB
  - Fully associative
    - Any VP can be placed in any PP
    - Requires a “large” mapping function – different from cache memories
  - Highly sophisticated, expensive replacement algorithms
    - Too complicated and open-ended to be implemented in hardware
  - Write-back rather than write-through
Enabling Data Structure: Page Table

- A **page table** is an array of page table entries (PTEs) that maps virtual pages to physical pages.
  - Per-process kernel data structure in DRAM
Page Hit

- **Page hit:** reference to VM word that is in physical memory (DRAM cache hit)

![Diagram of memory resident page table and virtual memory](image_url)
Page Fault

- **Page fault**: reference to VM word that is not in physical memory (DRAM cache miss)

![Diagram of page fault and memory management]

- Virtual address
  - Physical page number or disk address
    - Valid
      - 0: null
      - 1: Physical Memory (DRAM)
      - Memory resident page table (DRAM)
    - Physical Memory (DRAM)
      - VP 1
      - VP 2
      - VP 3
      - VP 4
      - VP 6
      - VP 7

- Virtual memory (disk)
  - VP 1
  - VP 2
  - VP 3
  - VP 4
  - VP 6
  - VP 7

- Physical memory (DRAM)
  - PP 0
  - PP 3
Handling Page Fault

- Page miss causes page fault (an exception)
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a victim to be evicted (here VP 4)

<table>
<thead>
<tr>
<th>Valid</th>
<th>Physical page number or disk address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>null</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>null</td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

**Memory resident page table (DRAM)**

**Physical memory (DRAM)**

- VP 1
- VP 2
- VP 7
- VP 4

**Virtual memory (disk)**

- VP 1
- VP 2
- VP 3
- VP 4
- VP 6
- VP 7
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a victim to be evicted (here VP 4)
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a victim to be evicted (here VP 4)
- Offending instruction is restarted: page hit!

**Key point:** Waiting until the miss to copy the page to DRAM is known as **demand paging**
Allocating Pages

Allocating a new page (VP 5) of virtual memory.

Physical page number or disk address

<table>
<thead>
<tr>
<th>Valid</th>
<th>PTE 0</th>
<th>PTE 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>null</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Virtual memory (disk)

- VP 1
- VP 2
- VP 3
- VP 4
- VP 5
- VP 6
- VP 7

Physical memory (DRAM)

- PP 0
  - VP 1
  - VP 2
  - VP 7
  - VP 3
- PP 3
  - VP 1
  - VP 2
  - VP 3
  - VP 4
  - VP 5
  - VP 6
  - VP 7
Locality to the Rescue Again!

- Virtual memory seems terribly inefficient, but it works because of locality.

- At any point in time, programs tend to access a set of active virtual pages called the **working set**
  - Programs with better temporal locality will have smaller working sets

- If \((\text{working set size} < \text{main memory size})\)
  - Good performance for one process after compulsory misses

- If \((\text{SUM(working set sizes)} > \text{main memory size})\)
  - **Thrashing**: Performance meltdown where pages are swapped (copied) in and out continuously
Today

- Address spaces
- VM as a tool for caching
- VM as a tool for memory management
- VM as a tool for memory protection
- Address translation
VM as a Tool for Memory Management

- **Key idea:** each process has its own virtual address space
  - It can view memory as a simple linear array
  - Mapping function scatters addresses through physical memory
    - Well-chosen mappings can improve locality

```
<table>
<thead>
<tr>
<th>Virtual Address Space for Process 1:</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP 1</td>
</tr>
<tr>
<td>VP 2</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>N-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Virtual Address Space for Process 2:</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP 1</td>
</tr>
<tr>
<td>VP 2</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>N-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Physical Address Space (DRAM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PP 2</td>
</tr>
<tr>
<td>PP 6</td>
</tr>
<tr>
<td>PP 8</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>M-1</td>
</tr>
</tbody>
</table>
```

(e.g., read-only library code)
VM as a Tool for Memory Management

- **Simplifying memory allocation**
  - Each virtual page can be mapped to any physical page
  - A virtual page can be stored in different physical pages at different times

- **Sharing code and data among processes**
  - Map virtual pages to the same physical page (here: PP 6)

Virtual Address Space for Process 1:

- VP 1
- VP 2
- ... (N-1)

Virtual Address Space for Process 2:

- VP 1
- VP 2
- ... (N-1)

Physical Address Space (DRAM):

- PP 2
- PP 6
- PP 8
- ... (M-1)

(e.g., read-only library code)
Simplifying Linking and Loading

**Linking**
- Each program has similar virtual address space
- Code, data, and heap always start at the same addresses.

**Loading**
- `execve` allocates virtual pages for `.text` and `.data` sections & creates PTEs marked as invalid
- The `.text` and `.data` sections are copied, page by page, on demand by the virtual memory system
Today

- Address spaces
- VM as a tool for caching
- VM as a tool for memory management
- VM as a tool for memory protection
- Address translation
### VM as a Tool for Memory Protection

- Extend PTEs with permission bits
- MMU checks these bits on each access

<table>
<thead>
<tr>
<th>Address Space</th>
<th>Physical Address Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>PP 2</td>
<td>PP 4</td>
</tr>
<tr>
<td>PP 4</td>
<td>PP 6</td>
</tr>
<tr>
<td>PP 6</td>
<td>PP 8</td>
</tr>
<tr>
<td>PP 8</td>
<td>PP 9</td>
</tr>
<tr>
<td>PP 9</td>
<td>PP 11</td>
</tr>
</tbody>
</table>

#### Process i:

<table>
<thead>
<tr>
<th></th>
<th>SUP</th>
<th>READ</th>
<th>WRITE</th>
<th>EXEC</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP 0:</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>PP 6</td>
</tr>
<tr>
<td>VP 1:</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>PP 4</td>
</tr>
<tr>
<td>VP 2:</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>PP 2</td>
</tr>
</tbody>
</table>

#### Process j:

<table>
<thead>
<tr>
<th></th>
<th>SUP</th>
<th>READ</th>
<th>WRITE</th>
<th>EXEC</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP 0:</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>PP 9</td>
</tr>
<tr>
<td>VP 1:</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>PP 6</td>
</tr>
<tr>
<td>VP 2:</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>PP 11</td>
</tr>
</tbody>
</table>
Today

- Address spaces
- VM as a tool for caching
- VM as a tool for memory management
- VM as a tool for memory protection
- Address translation
VM Address Translation

- Virtual Address Space
  - $V = \{0, 1, \ldots, N-1\}$

- Physical Address Space
  - $P = \{0, 1, \ldots, M-1\}$

- Address Translation
  - $\text{MAP}: V \rightarrow P \cup \{\emptyset\}$
  - For virtual address $a$:
    - $\text{MAP}(a) = a'$ if data at virtual address $a$ is at physical address $a'$ in $P$
    - $\text{MAP}(a) = \emptyset$ if data at virtual address $a$ is not in physical memory
      - Either invalid or stored on disk
Summary of Address Translation Symbols

- **Basic Parameters**
  - $N = 2^n$: Number of addresses in virtual address space
  - $M = 2^m$: Number of addresses in physical address space
  - $P = 2^p$: Page size (bytes)

- **Components of the virtual address (VA)**
  - TLBI: TLB index
  - TLBT: TLB tag
  - VPO: Virtual page offset
  - VPN: Virtual page number

- **Components of the physical address (PA)**
  - PPO: Physical page offset (same as VPO)
  - PPN: Physical page number
Address Translation With a Page Table

Virtual address

Virtual page number (VPN)  Virtual page offset (VPO)

Page table

Valid  Physical page number (PPN)

Valid bit = 0: Page not in memory (page fault)

Valid bit = 1

Physical page number (PPN)  Physical page offset (PPO)

Physical address

Page table base register (PTBR) (CR3 in x86)

Physical page table address for the current process

Valid bit = 0: Page not in memory (page fault)
Address Translation: Page Hit

1) Processor sends virtual address to MMU
2-3) MMU fetches PTE from page table in memory
4) MMU sends physical address to cache/memory
5) Cache/memory sends data word to processor
Address Translation: Page Fault

1) Processor sends virtual address to MMU
2-3) MMU fetches PTE from page table in memory
4) Valid bit is zero, so MMU triggers page fault exception
5) Handler identifies victim (and, if dirty, pages it out to disk)
6) Handler pages in new page and updates PTE in memory
7) Handler returns to original process, restarting faulting instruction
Integrating VM and Cache

VA: virtual address, PA: physical address, PTE: page table entry, PTEA = PTE address
Speeding up Translation with a TLB

- Page table entries (PTEs) are cached in L1 like any other memory word
  - PTEs may be evicted by other data references
  - PTE hit still requires a small L1 delay

- Solution: *Translation Lookaside Buffer* (TLB)
  - Small set-associative hardware cache in MMU
  - Maps virtual page numbers to physical page numbers
  - Contains complete page table entries for small number of pages
Accessing the TLB

- MMU uses the VPN portion of the virtual address to access the TLB:

  TLBT matches tag of line within set

  TLB tag (TLBT)  TLB index (TLBI)  VPO

  T = 2^t sets

  n-1  p+t  p+t-1  p  p-1  0

  TLBI selects the set

  Set 0

  Set 1

  Set T-1
A TLB hit eliminates a memory access
A TLB miss incurs an additional memory access (the PTE)
Fortunately, TLB misses are rare. Why?
Multi-Level Page Tables

- **Suppose:**
  - 4KB \(2^{12}\) page size, 48-bit address space, 8-byte PTE

- **Problem:**
  - Would need a 512 GB page table!
    - \(2^{48} \times 2^{-12} \times 2^3 = 2^{39}\) bytes

- **Common solution:** Multi-level page table

- **Example:** 2-level page table
  - Level 1 table: each PTE points to a page table (always memory resident)
  - Level 2 table: each PTE points to a page (paged in and out like any other data)
We have a problem

2^{20} Entries of 4 bytes each

32 bit addresses, 4KB pages, 4-byte PTEs

Virtual memory

0

VP 0
...
VP 1023
VP 1024
...
VP 2047

2K allocated VM pages for code and data

Gap

6K unallocated VM pages

1023 unallocated pages

1 allocated VM page for the stack

1023 unallocated pages

PTE 9215

(null)

(null)

(null)

VP 9215
A Two-Level Page Table Hierarchy

Level 1
page table

- PTE 0
- PTE 1
- PTE 2 (null)
- PTE 3 (null)
- PTE 4 (null)
- PTE 5 (null)
- PTE 6 (null)
- PTE 7 (null)
- PTE 8
- (1K - 9) null PTEs

Level 2
page tables

- PTE 0
- ... PTE 1023
- PTE 0
- ... PTE 1023
- 1023 null PTEs
- PTE 1023

Virtual memory

- VP 0
- ... VP 1023
- VP 1024
- ... VP 2047
- Gap
- 1023 unallocated pages
- VP 9215
- 1023 unallocated VM pages
- 2K allocated VM pages for code and data
- 6K unallocated VM pages
- 1 allocated VM page for the stack

32 bit addresses, 4KB pages, 4-byte PTEs
Translating with a k-level Page Table

- Page table base register (PTBR)
- Virtual address space
  - Level 1 page table
  - Level 2 page table
  - Level k page table

- Physical address space
  - PPN
  - PPO
Summary

- **Programmer’s view of virtual memory**
  - Each process has its own private linear address space
  - Cannot be corrupted by other processes

- **System view of virtual memory**
  - Uses memory efficiently by caching virtual memory pages
    - Efficient only because of locality
  - Simplifies memory management and programming
  - Simplifies protection by providing a convenient interpositioning point to check permissions
Harry is having trouble with getopt on cachelab and googles for getopt to see how to use it.

Jane is having trouble with fscanf on cachelab and talks to a friend about how to use it. Her friend shows her an example for reading two integers from a file.

Sam is confused about how a cache works and goes to wikipedia to learn about caches. He googles for “cache.” He reads several web pages and then starts to write his code.
Academic Integrity “Refresher”

- Joe has spent several hours staring at a blank sheet of paper and doesn’t know how to get started. He googles for “cachelab” and finds a blog online which talks about how caches work. He reads it and then implements the code on his own.

- Mary, after several frustrating days, googles for caches and comes across a github page with the code for cachelab. She looks at the code. Then she closes her browser and implements the code on her own.
Academic Integrity “Refresher”

- Frank is stuck and talks to his friend about whether he should use multiple arrays or an array of structures. They don’t look at code together.

- Andre is stuck and talks to a TA about that fields he should use to represent a cacheline. They are working together and writing things down on a piece of paper.

- Laura is stuck and talks to a friend about that fields she should use to represent a cacheline. They don’t write anything down.