Memory Spot:
A Labeling Technology

More than 15 times faster than existing RFID technologies, the batteryless Memory Spot system supports reading, writing, and appending of megabytes of digital content.

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One challenge facing the Internet of Things[1,2] is labeling physical objects to let them participate in the digital world. Until now, most solutions addressed this issue by using either 1D or 2D bar codes or RFID.[3] Such RFID devices include the 2.4-GHz Hitachi μ-chip,[4] the widely deployed 13.56-MHz Mifare (http://mifare.net) and Felica (www.sony.net/Products/felica) systems, and the Near Field Communication technology that the NFC Forum (www.nfc-forum.org) is developing.[5,6]

The μ-chip and NFC devices support read operations of only small data amounts (tens of bits) and thus are constrained to referential data access. Mifare, Felica, and NFC tags can contain many kilobytes of memory but have limited data rates. Access times for more than 100 Kbytes can be too long for a "tap-and-go" experience, so these labels typically contain only a reference to the content associated with the physical object. To access that content, the system must resolve the reference and fetch the content from a remote database. This solution has potential disadvantages. Server and network latencies detract from the user experience and prevent interaction with the application if the response is slow. Maintaining wireless network coverage is also difficult, and the cost of downloading megabytes of content can rapidly become prohibitive.

Our Memory Spot system addresses these issues, storing relatively large amounts of rich content on the actual physical object—called *nonreferential storage*. To minimize user interaction time, Memory Spot's on-air data rate is 10 Mbits per second (Mbps)—substantially higher than conventional RFID data rates.

Technical Background

Memory Spot's primary design goal is fast access to content, such as documents, images, and audio clips, that require memory capacity ranging from tens of kilobytes to megabytes. Rapidly accessing this much content requires high system throughput; again, we chose 10 Mbps for the applications envisaged. To ensure a good user experience, we require unambiguous access to content and therefore desire a short (less than 2 mm) or actually touching interaction range.

System Design

Memory Spot's system hardware comprises the Memory Spot chip and its reader/writer. Figure 1 illustrates each component's form factor and sizes, with the tiny chip just visible under the reader/writer's tip in Figure 1a. To meet our goals for system throughput and ease of use, we chose the 2.4-GHz Industry, Science, Medicine (ISM) band for the wireless interface because it offers sufficient bandwidth

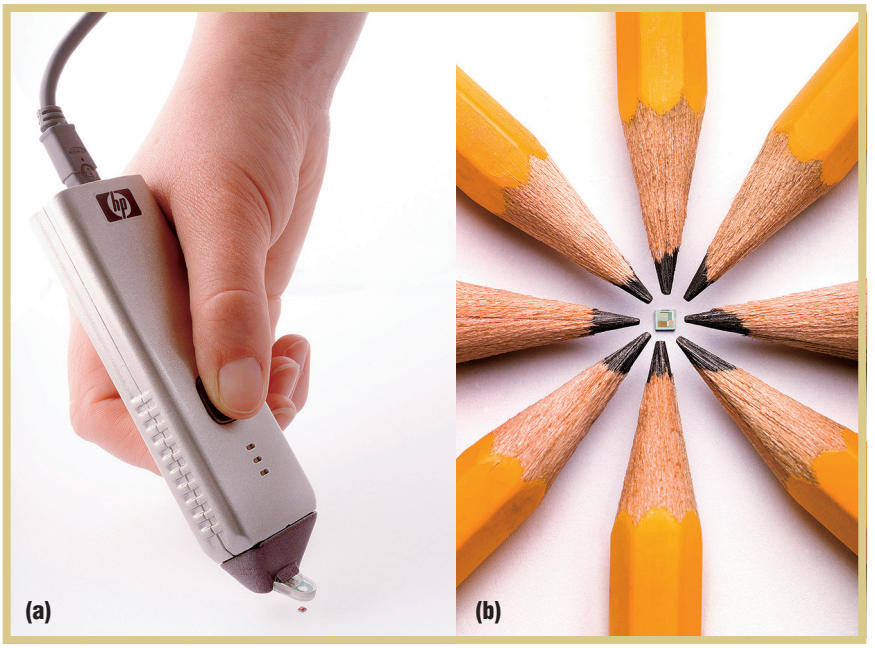

Figure 1. The Memory Spot (a) reader/writer and (b) chip. The user brings the reader/writer, a handheld USB device, in close proximity of the chip to initiate reading, writing, and appending of content. The chip is often encased in a 10-mm diameter self-adhesive package.

to support our high data rate without complex multilevel modulation schemes. A 2.4-GHz antenna is also small enough to support unambiguous interaction between the reader/writer and chip.[7,8]

Because the reader/writer inductively powers the chip, power transfer efficiency between the two is critical. Our current design operates with a 10-dB coupling loss. With a transmit power of 70 mW, which is within allowable power limits for most geographic regions, and with a 40 percent rectification efficiency, the chip has approximately 3 mW of power available to support its read and write operations. Its wireless modem uses less than 1 mW of this available power; its memory uses the remaining 2 mW.

The reader/writer transfers data to the chip using amplitude modulation with a modulation depth between 10 and 20 percent. This provides well-separated modulation states for robust communication while avoiding excessive ripple in the instantaneous transmitted power. To allow clock recovery using only low-cost (in power and silicon area) techniques, we use Manchester coding on the data, which results in a 5-Mbps information rate. In addition, we added duo-binary phase modulation to the transmitted signal to spread the spectrum. This reduces the transmission's power spectral density to a level that meets regional government regulations, such as those of the US Federal Communications Commission (FCC). We designed the phase modulation to operate independently of the data-bearing amplitude modulation to enable a simple receiver architecture. The power envelope is the same whether or not we use phase spreading. The chip uses a load modulation technique to transfer the data, which is detected by the reader/writer's phase detector. Manchester coding isn't necessary on this link, so we can achieve the full 10-Mbps data rate. Because the chip needs power during this transaction, the reader/writer must continue to transmit, and the transmission must comply with local regulations. This means that, in many cases, we will have to use phase modulation.

Because of the high-Q nature of the inductive coupling between the chip and the reader/writer, phase modulation can cause phase detector output amplitude distortions that degrade the recovered data signal from the chip. A simple but effective way to deal with this is to first train the reader/writer with a representative signal portion incorporating the phase modulation—but no data from the chip.[9] You then use that training to remove the distortion once the reader/writer starts receiving the data.

The Memory Spot Chip

The chip is a complementary metal-oxide semiconductor (CMOS) memory device, with integrated wireless data I/O and power transfer complete with an on-chip antenna.[10] It has five subsystems: antenna, modem, processor, security engine, and memory. The chip incorporates the 10-Mbps wireless interface operating in the global unlicensed 2.4-GHz ISM band. Powered by the reader/writer, it requires no external electronics or batteries. We designed two chips using an industry-standard 0.18-μm process with read/write flash memory of 32 and 512 Kbytes.

We anticipate that all future volume products based on the Memory Spot architecture will use process technologies smaller than 0.18 μm. This lets us support larger memory sizes—1 Mbyte and more—while minimizing the silicon area. Although a complete Memory Spot chip has a larger silicon area (to support its large memory capacity) than similar memory devices, its overall cost is comparable because its packaging costs are lower. For a Memory Spot chip with an integrated antenna, there are no external antenna costs to consider, and the off-chip antenna structure is usually smaller and simpler than an equivalent 13.56-MHz antenna, thus reducing its cost.

Through careful choice of system architecture and low-power design, we accommodated the necessary high-speed memories while minimizing our transmitted power requirements. Our modem and on-chip processor consume less than 1 mW operating at 10 Mbps, with the processor providing an equivalent processing power of some 340 million operations per second (MOPS). The modem and processor use approximately 0.66 mm^2 of silicon.

The 2.4-GHz loop antenna receives wireless power from the reader/writer and transmits and receives data. The antenna is integrated in the chip to achieve the smallest size, the lowest cost, and increased reliability.[11] Inductive coupling at 2.4 GHz transfers power between a reader/writer device and the chip's integrated circuit (IC). The reader/writer has a single-turn coil of approximately 3-mm diameter that couples to a single-turn coil on the IC, fabricated around the periphery of the 32-Kbyte chip.

The chip's protocol processor has a single clock per machine cycle and can process bit streams.[12] The core has two levels. Level 1 is basically a stripped-down RISC (reduced-instruction-set computing) architecture, which deals with commands that affect the instruction pointer, such as conditional jumps. It adopts a modified Harvard-type architecture with separate 33-bit instruction and two data buses running at full speed to execute programs and access data from both on-chip and external memory. The design, optimized for data communication, allows access to up to eight conditions simultaneously and updates the instruction pointer in a single clock cycle. Level 2 contains reconfigurable blocks commonly used in data communications, such as a correlator and checksum calculator. All functional blocks in levels 1 and 2 can operate in parallel, resulting in up to 34 operations per clock cycle. The processor has 20 8-bit registers, nine of which can be accessed directly by the operation codes.

The program memory and processor core use 0.29 mm^2 of silicon area; again, the power consumption at full speed is less than 1 mW. We implemented three variants of the protocol processor for testing. Each processor targets a different memory technology: on-chip RAM with external battery backup, on-chip mask ROM, and externally addressed FRAM (ferroelectric RAM).

For demonstration purposes, we packaged Memory Spot chips in self-adhesive roundels of 10-mm diameter. Users can peel these chips off their backing sheet and apply them to documents, photographs, medicine bottles, equipment, and so forth.

The Reader/Writer

Memory Spot's reader/writer is an advanced prototype. Two versions are available: one powered by a mains-based adaptor and a battery-powered version for mobile applications. Both types present a USB interface, use an IP-based control and data protocol, and incorporate low-power ARM processors in a form that's slightly larger than a fluorescent highlighter pen.

For optimum coupling to chips incorporating an antenna, the reader/writer's antenna is a simple coil approximately 3 mm in diameter that's impedance-matched to the reader/writer via two low-loss capacitors. The chip antenna's Q factor is approximately 12, its losses due to the antenna track resistance and eddy currents induced in the underlying silicon substrate. The reader/writer antenna performs considerably better, with a Q factor approaching 100. This combination of antenna loops, when operated in close proximity of approximately 1 mm, results in a coupling factor of about 0.015. This produces (when accounting for the other antenna-matching circuits' component losses) the 10-dB coupling loss we mentioned earlier.

Bringing the reader/writer's tip close to the chip to interact with it is intuitive. The relatively close operating range means that no ambiguity exists about which chip the reader/writer is interrogating.

The Communication Protocol

We developed a protocol to support efficient communication between the reader/writer and chip. With careful antenna system design, we achieved an entirely intuitive tap-and-go use model to read and write content. Memory Spot shifts most of the communications management burden to the reader/writer, which doesn't have the chip's power and size constraints. The rapid link establishment and data transfer phases begin after the reader/writer energizes the chip; the session terminates when the reader/writer drops power to the chip.

Our modem and on-chip processor consume less than 1 mW operating at 10 Mbps, with the processor providing an equivalent processing power of some 340 MOPS.

Memory Spot's structure causes several constraints on the communications protocol. Because of the efficiency of the reader/writer's inductive power transfer, the chip must consume minimal power. So, it must use the minimal number of logic gates to behave like a serial-access memory device and can't, for example, buffer incoming data for subsequent processing. Memory Spot

currently assumes that a given chip is at least 2 mm away from another spot. This means that we can simplify the protocol to avoid an enumeration and addressing phase in RFID when multiple chips are in the reader/writer's field of view.

During the communications session, the chip responds to each command from the reader/writer with a positive or negative acknowledgment. The variable-size payload lets the chip transmit a data packet in the presence of significant amounts of noise. However, the reader/writer must make operational trade-offs when noise is present because a single byte of transmitted data requires an overhead of 15 bytes. In a typical environment containing traffic from Wi-Fi access points, Bluetooth, and other 2.4-GHz ISM band users, Memory Spot chips routinely use packet sizes of several tens of kilobytes. The reader/writer requests packet sizes for data coming from the chip and can apply similar control to achieve a balance between robustness and throughput.

We've also been able to accommodate an established NFC protocol in our architecture. In December 2009, Ecma International released ECMA-391, a 2.4-GHz NFC interface and protocol standard based on the Memory Spot system (see www.ecma-international.org/publications/standards/ECMA-391.htm). This standard leverages the Ecma NFCIP-1 specification's transport protocol, ECMA-340, also called ISO/IEC 18092 (www.ecma-international.org/publications/standards/ECMA-340.htm).

Security Features

Memory Spot's standard security features include a unique ID, anticloning system, and 28-byte password that restricts read access, which users can switch off if not required. The challenge response mechanism validates Memory Spot and is used in conjunction with a remote database in secure applications, such as pharmaceutical anticounterfeiting.[13]

Memory Spot's 32 or 512 Kbytes of memory are sufficient for high-resolution images of protected products or medicine (called *fingerprints*) and full product provenance, an expiration date, and a digital signature to ensure data authenticity. In this way, Memory Spot can deliver local, digitally signed, trusted content. The chips are physically small (approximately 2 mm^2 in area and 0.3 mm thick) and can be fitted securely and unobtrusively into something as small as a vial, blister pack, or pill bottle seal. The access range is physically restricted to less than 2 mm, so shielding the chip to prevent reading or writing until the packaging is actually broken is reasonably easy. A unique factory-programmed ID that's difficult to modify and an onboard challenge response authenticator (based on the standard cryptographic primitive SHA-1 with 16 224-bit keys) defend against cloning and impersonation attacks.

Memory Spot's standard security features include a unique ID, anticloning system, and 28-byte password that restricts read access.

Secure applications, such as asset protection, use hard WORM (write-once, read-many) memory to guarantee nonerasable, nonmodifiable access history or manufacturer data. Soft (simulated) WORM technology that lets users configure the WORM size after manufacture is generally less secure and more expensive. The organization specifying the solution usually knows the required WORM size before manufacture for the intended applications, such as detection of counterfeit medicine, and these applications don't require users to reconfigure WORM.

We adopted hard WORM for these cost and security reasons. Current RFID devices similar to Memory Spot in cost and size don't support strong cryptographic primitives because of their complexity; various major manufacturers have adopted less secure stream-based algorithms instead.

Memory Spot Applications

Memory Spot's ability to store a comparatively large amount of data enables many possible pervasive applications. These applications need to access large amounts of data rapidly and support multimedia content with typical object sizes of 1 to 2 Mbytes, with the expectation that object sizes will increase in the future. The consumer and enterprise applications we outline here require a download speed of 10 Mbps or more; existing high-speed technologies, such as EPC Global Gen2, can't support them adequately.[14] Although many of the applications are currently prototypes, we intend to implement constrained user trials to field-test the concepts.

Dynamic Preroll and Interlude Videos

When dealing with streaming media in mobile applications (for example, a media-enriched tourist attraction), appropriately managing the connection setup and buffering can be the difference between a seamless or a disjointed user experience. A client device can display a blank screen, static logo, or progress bar of indeterminate length while it's setting up a connection and buffering the streaming media. However, such approaches can discourage people from using these services.

By leveraging Memory Spot's physical colocation, storage capacity, and fast read times, an application can

- store a *preroll video*—a short video that plays before the main feature—which could contain an abstract or content highlights;
- deliver it to the device for playback in a fraction of a second; and
- provide the client with instantaneous, valuable content while the device is setting up the connection and buffering the main feature.

Unlike a typical cache, preroll videos are generated dynamically from a script and set of resources, and therefore have varying lengths. The preroll video's dynamism is critical because the time necessary to set up the streaming connection and fill the buffer depends on many network and environmental factors. Combining a frame server client on the device with a script and stored resources on Memory Spot, the application can render, deliver, and gracefully splice the video into the main feature as it becomes available. The video is typically a text-rich presentation with a set of audio and video resources, limited only by the Memory Spot chip's size and the nature of the main feature.

This approach also works for mid-video interludes. Memory Spot can dynamically create an interlude video that can be mixed in gracefully and displayed while buffering and reconnect occur in the background. In this way, it provides the user with a much less jarring experience than a typical "connection failed" or "buffering, please wait" message.

Many devices, such as typical audio guides, store all media locally. However, such an approach has two drawbacks. First, storing the media on the device renders the experience static—that is, the content can't churn. In some cases, this isn't a problem, but for more interactive applications—especially those that encourage user feedback and contribution—the content life cycle must be dynamic. Combining a read- and write-enabled Memory Spot and streaming media produces a substantially more dynamic content life cycle. Second, such devices have limited storage, and caching the entire content library on each device typically constrains the scope to a single location. With combined colocated cached data and network-based media, a single client device is applicable at multiple locations without additional processor management overhead.

Asset Annotation

Adding local digital content to an asset can facilitate physical asset annotation. This is particularly true in situations in which an infrastructure either doesn't exist or has been destroyed, precluding the use of conventional by-reference technologies, wherein data is stored in a remote database. Example scenarios are humanitarian relief efforts for natural disasters and peacekeeping operations in remote areas.

On interrogation, the asset can immediately present a description of itself and its provenance (or selected parts of it) to an authorized reader. For example, Memory Spot could store an asset's product description, user manual, warranty information, maintenance history, and recycling information. Memory Spot's journaling mode can also append updates to an asset's maintenance history and simultaneously log the updates in the reader/writer, which can synchronize with a master database once the reader/writer connects to a back-end infrastructure.

> Currently, developers have two options for user-interaction platforms interfacing to the reader/writer—one based on a laptop and the other on a PDA.

Urban YouTube

Another compelling application lets users download and store a YouTube-like video to Memory Spot. Users can attach the video to an object, such as a wall or digital graffiti space, in the same way they leave a written Post-it note in a public space, such as a desk or book, for friends to access. The largest memory size we've used is 0.5 Mbyte, affording tantalizing glimpses of what's possible with larger memories (more than 2 Mbytes) when we move the technology to smaller process geometries and more exotic memories.

Dual-Port Memory Spot

We can extend Memory Spot's chip by incorporating a wired interface into the onboard memory. In effect, Memory Spot becomes a dual-port device with both a wired and wireless interface. This configuration enables a novel application, letting manufacturers install last-minute firmware patches wirelessly in a host device, such as a printer, when it's powered off and in its shipping box. When the host device ultimately powers up, the host processor interrogates Memory Spot over the wired connection and installs the patch. This concept extension requires longer-range reader/writer antennas, an external long-range (20 cm) antenna on the chip, and careful consideration of the security implications. Even so, it has obvious benefits for production environments, just-in-time configuration, and product personalization.

Current Status

Memory Spot R&D has been ongoing for several years at HP Labs. We can now demonstrate a complete system

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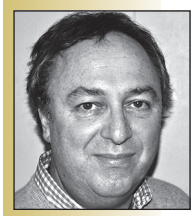

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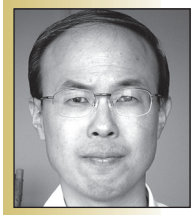

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with applications using the battery-powered reader/writer. We're also planning limited technology proofs of concept in asset management.

We created a software developer's kit (SDK) that simplifies and accelerates client-side application development. The SDK provides a set of .NET libraries that make interacting with the reader/writer and chip trivial. Sample applications showcase Memory Spot's capabilities and demonstrate the ease with which clients can develop applications and prototypes with our SDK.

Currently, developers have two options for user-interaction platforms interfacing to the reader/writer—one based on a laptop and the other on a PDA (HP iPAQ). Because it's not constrained by processor power, screen size, and battery, the laptop allows more flexible interaction with Memory Spot applications. However, it isn't a handheld solution. The iPAQ-based solution overcomes this problem, but its relatively small screen limits screen-based interactions, especially in data-rich applications such as asset management. Another shortcoming is that holding the reader/writer and the iPAQ occupies both hands, leading some people to use the reader/writer's tip as a stylus—which works but wasn't our intention.

The initial findings from user trials convinced us that a fully integrated solution on a smart phone platform is the ultimate design objective. A smart phone is a perfect I/O and capture device for applications we're targeting. We estimate that the reader/writer will share 80 percent of an 802.11 wireless local-area-network (WLAN) system, so the silicon real estate increase would be minimal when implementing our reader/writer.

Future work under consideration includes increasing the on-air data rate capability to accommodate Memory Spot's anticipated larger memory

sizes. The reader/writer's dwell time over the chip must be sufficiently short so as not to become an issue for the user. So, larger memories will require on-air data rates of 40 Mbps and more, which creates some technical challenges. At 20 Mbps, the bandwidth available at 2.4 GHz will still permit simple two-level modulation schemes. However, at higher data rates, complex multilevel modulation techniques might be necessary. This will require very-low-power modems that operate from the power supply derived from the magnetic coupling between the reader/writer and the chip. High-speed nonvolatile memories with lower power requirements will also be required. P

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