Logic Emulation Technology

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Background

- The Original Killer App
  - IC simulation: Hz -> kHz
  - $$$$
- Quickturn Systems
  - Xilinx FPGAs, 2D Mesh interconnect
  - Problems?

PLASMA Architecture

- Hextant Xbar:
  - nearly fully populated
  - 100 pins output from Hextant
    - Rent Exponent?
- Central Xbar:
  - 1600 inputs
  - 1/4 populated.
- 336 IOs for 256 6-LUTs!
  - Rent prediction: 128 IOs (exponent = 0.5)

Register Files

- Register Files
  - Multiple write-port Regfiles hard in exisitng FPGAs
  - Necessary for CPU emulation
- 40 PALEs -> 1 bit reg file
  - 64 words
  - 8 read ports
  - 8 write ports

Teramac Architecture

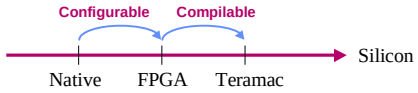
- MCMs: 27 PLASMAs each
- Boards: four MCMs
- 4800 connections per board

Teramac CAD

- Use design specification hierarchy
- P&R by recursive bi-partitioning
- Performance
  - 2 seconds per chip
  - 1 minute per MCM
  - 5 minutes per board
    - ~30,000 LUTs in 5 minutes

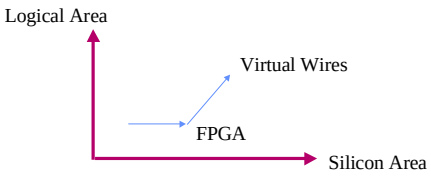
Teramac Philosophy

- WIRES! WIRES! WIRES!
- Fast compilation at any hardware cost
- Reconfigurable computing?



Virtual Wires

- Chip IOs: The big bottleneck
  - Internal FPGAs under-utilized
- Modify logic design
  - One emulation cycle:
    - Multiple phases, why?
    - 100s of µClks
- First case of “true” hardware virtualization
  - Time-multiplex physical pins

Virtual Wires Philosophy

- More logic to get around pin limitation