

VLSI Devices and Fabrication

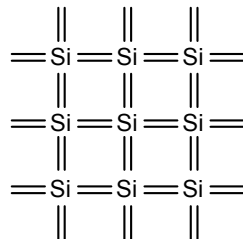
Seth Copen Goldstein
seth@cs.cmu.edu
CMU

Admin

- Include name, andrewid, date, article title on handins.
- Ok, good, see me
- If you want to work on your english ...

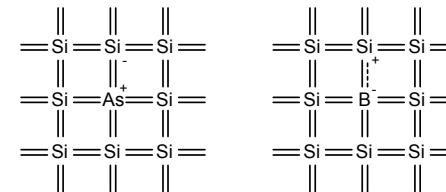
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



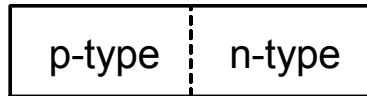
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

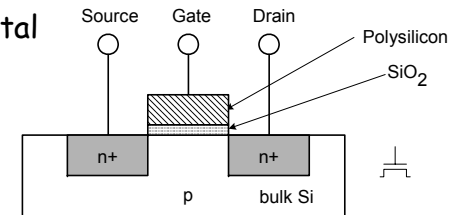


anode cathode



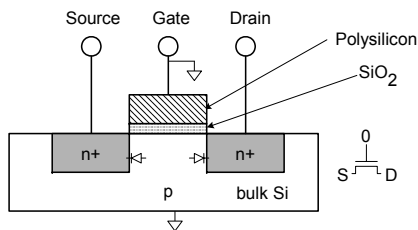
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate - oxide - body stack looks like a capacitor
 - Gate and body are conductors
 - SiO_2 (oxide) is a very good insulator
 - Called metal - oxide - semiconductor (MOS) capacitor
 - Even though gate is no longer made of metal



nMOS Operation

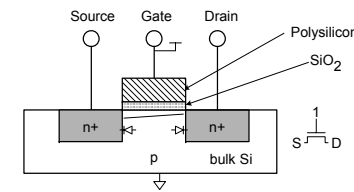
- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
 - P-type body is at low voltage
 - Source-body and drain-body diodes are OFF
 - No current flows, transistor is OFF



nMOS Operation Cont.

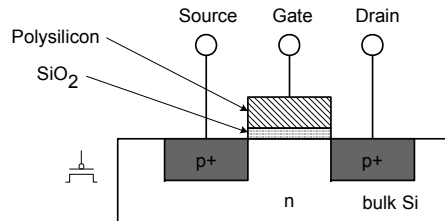
When the gate is at a high voltage:

- Positive charge on gate of MOS capacitor
- Negative charge attracted to body
- Inverts a channel under gate to n-type
- Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
 - Body tied to high voltage (V_{DD})
 - Gate low: transistor ON
 - Gate high: transistor OFF
 - Bubble indicates inverted behavior

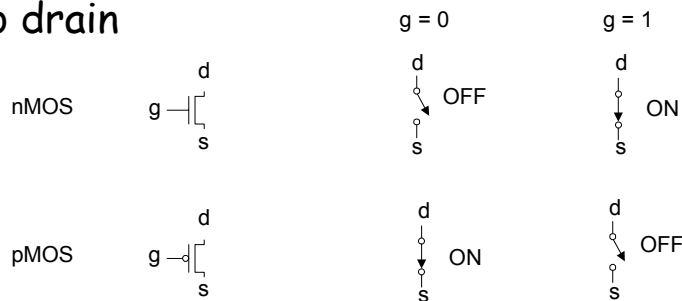


Power Supply Voltage

- $GND = 0 V$
- In 1980's, $V_{DD} = 5V$
- V_{DD} has decreased in modern processes
 - High V_{DD} would damage modern tiny transistors
 - Lower V_{DD} saves power
- $V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, \dots$

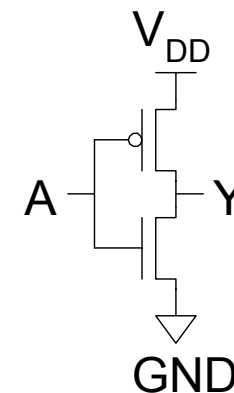
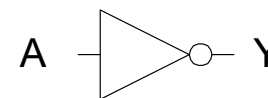
Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



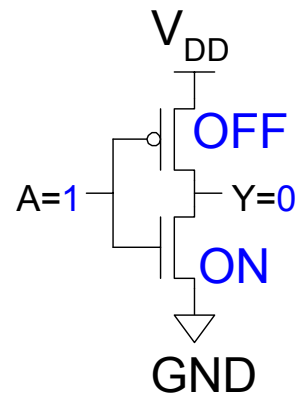
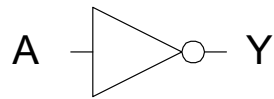
CMOS Inverter

| A | Y |
|---|---|
| 0 | |
| 1 | |



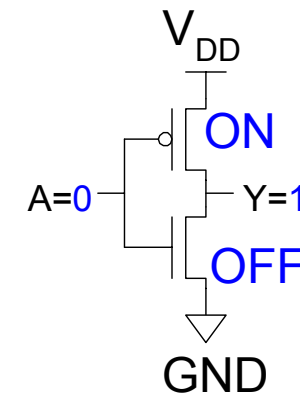
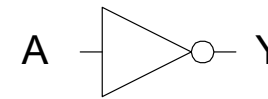
CMOS Inverter

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |



CMOS Inverter

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

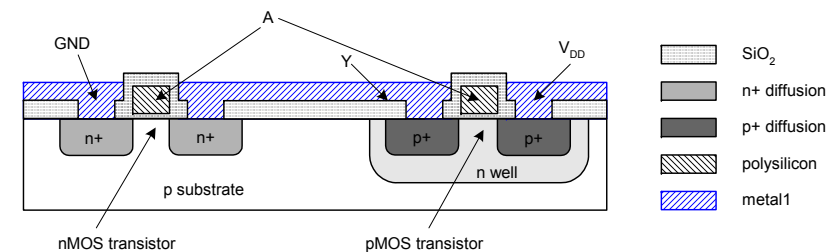


CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

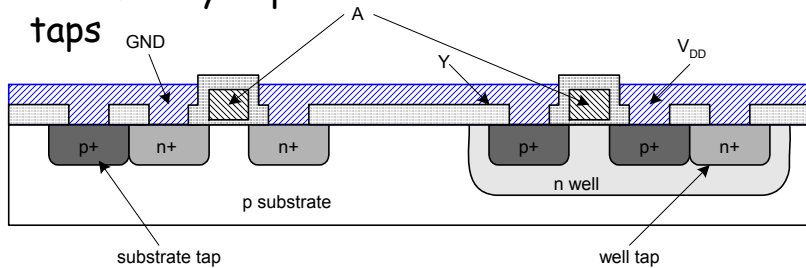
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



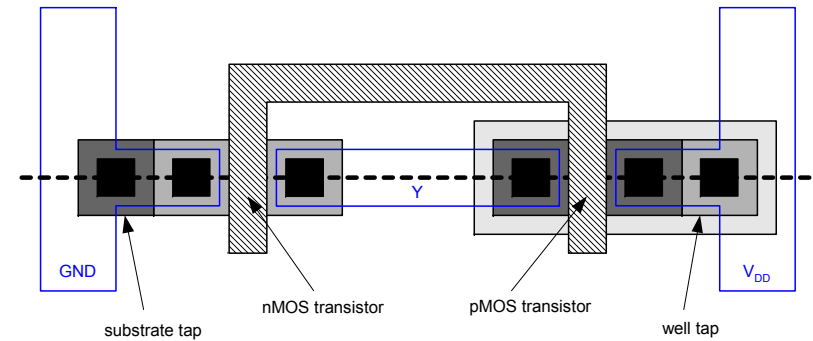
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



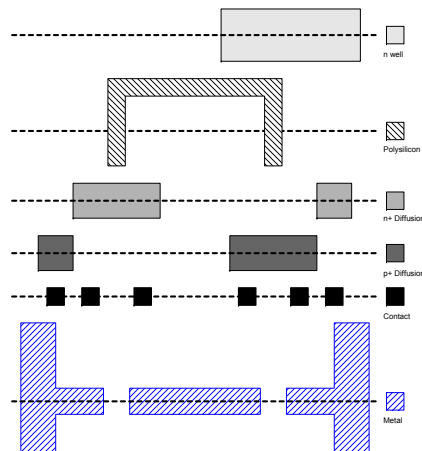
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
 - n-well
 - Polysilicon
 - n+ diffusion
 - p+ diffusion
 - Contact
 - Metal



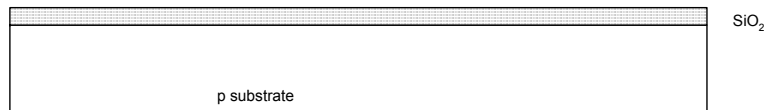
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
 - Cover wafer with protective layer of SiO_2 (oxide)
 - Remove layer where n-well should be built
 - Implant or diffuse n dopants into exposed wafer
 - Strip off SiO_2



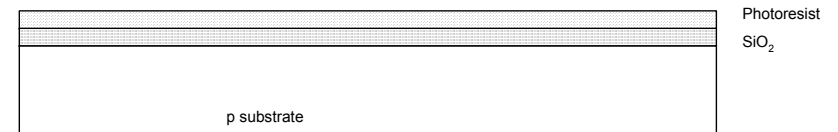
Oxidation

- Grow SiO_2 on top of Si wafer
 - 900 - 1200 C with H_2O or O_2 in oxidation furnace



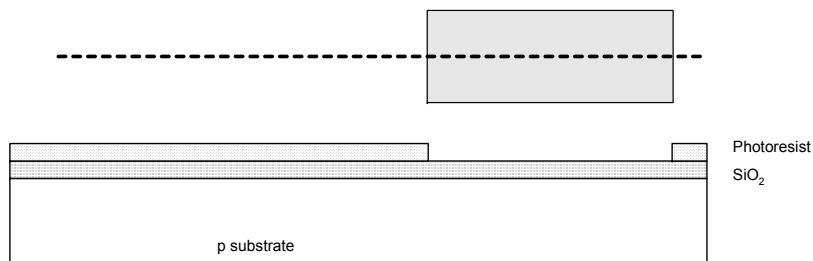
Photoresist

- Spin on photoresist
 - Photoresist is a light-sensitive organic polymer
 - Softens where exposed to light



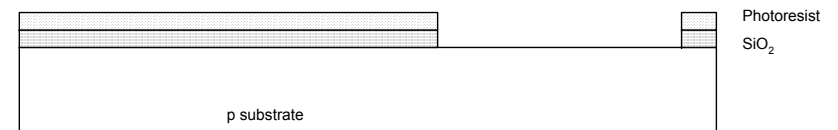
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



Etch

- Etch oxide with hydrofluoric acid (HF)
 - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



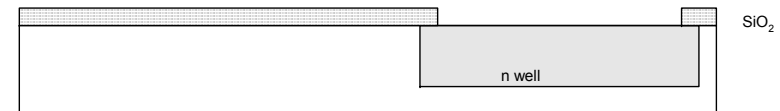
Strip Photoresist

- Strip off remaining photoresist
 - Use mixture of acids called piranha etch
- Necessary so resist doesn't melt in next step



n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
 - Place wafer in furnace with arsenic gas
 - Heat until As atoms diffuse into exposed Si
- Ion Implantation
 - Blast wafer with beam of As ions
 - Ions blocked by SiO₂, only enter exposed Si



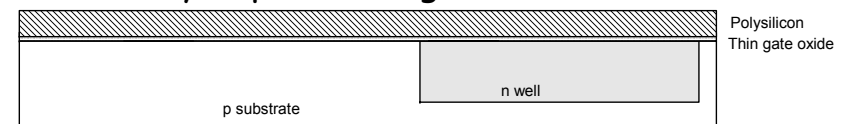
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



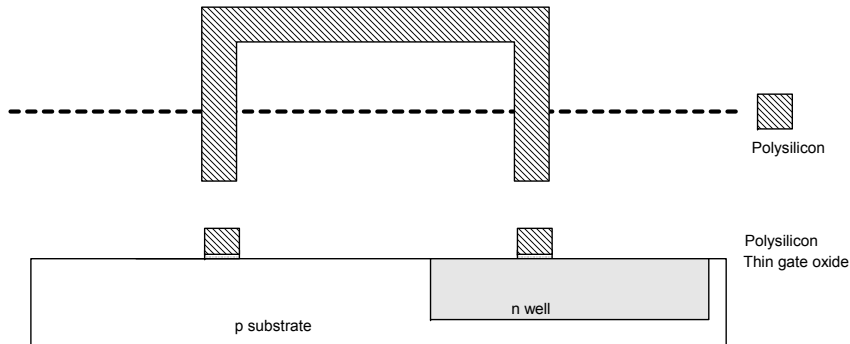
Polysilicon

- Deposit very thin layer of gate oxide
 - $< 20 \text{ \AA}$ (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
 - Place wafer in furnace with Silane gas (SiH₄)
 - Forms many small crystals called polysilicon
 - Heavily doped to be good conductor



Polysilicon Patterning

- Use same lithography process to pattern polysilicon



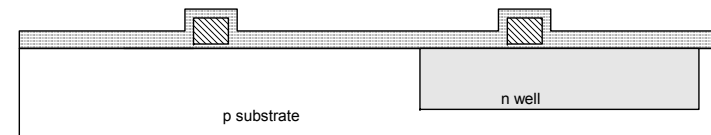
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Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



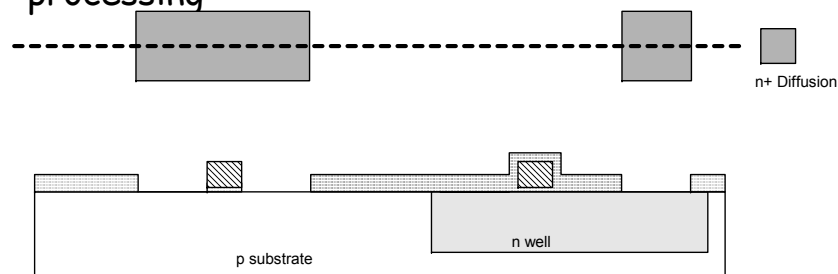
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N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



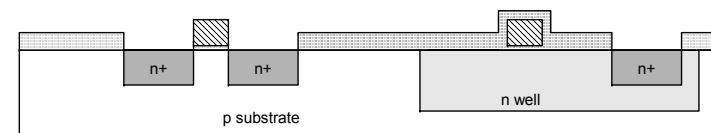
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N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



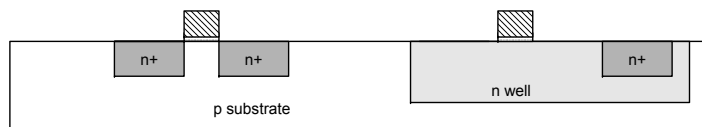
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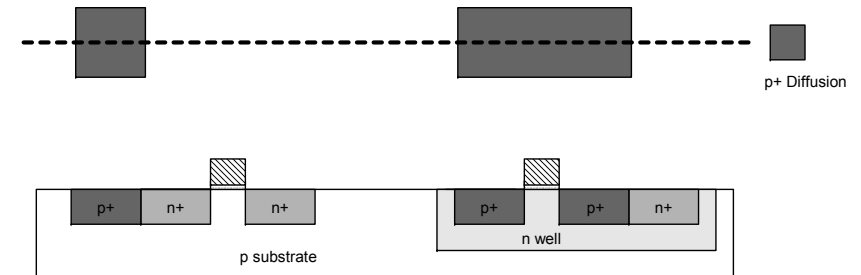
N-diffusion cont.

- Strip off oxide to complete patterning step



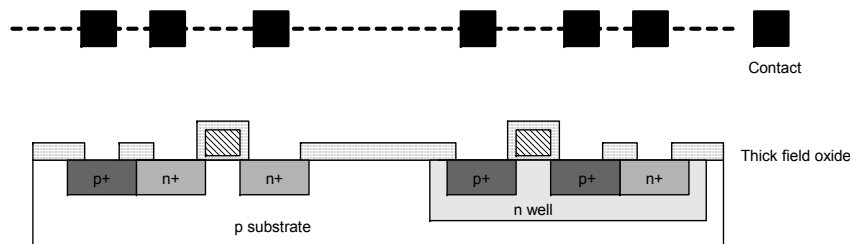
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



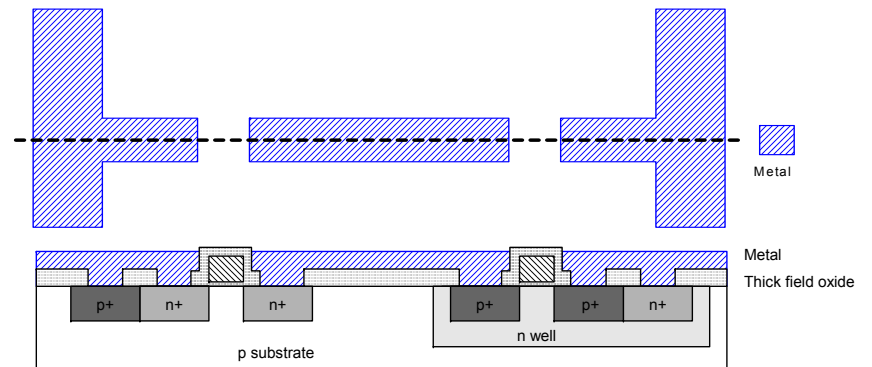
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Polysilicon Refining

Chemical Reactions

Silicon Refining: $\text{SiO}_2 + 2 \text{C} \rightarrow \text{Si} + 2 \text{CO}$
 Silicon Purification: $\text{Si} + 3 \text{HCl} \rightarrow \text{HSiCl}_3 + \text{H}_2$
 Silicon Deposition: $\text{HSiCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3 \text{HCl}$

Reactants

H_2

Silicon Intermediates

H_2SiCl_2

HSiCl_3



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Crystal Pulling

Process Conditions

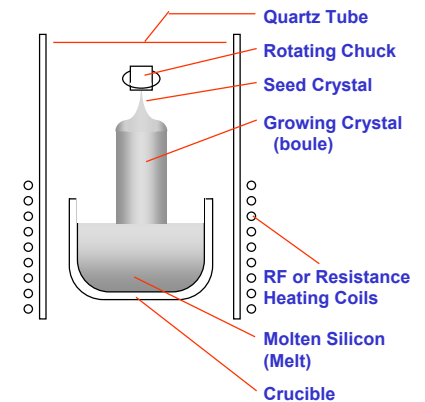
Flow Rate: 20 to 50 liters/min
 Time: 18 to 24 hours
 Temperature: >1,300 degrees C
 Pressure: 20 Torr

Materials

Polysilicon Nodules *

Ar *

H_2

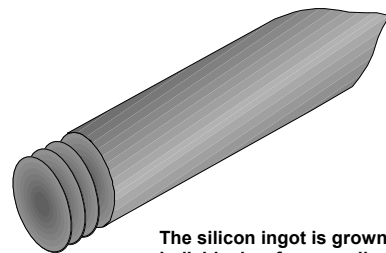
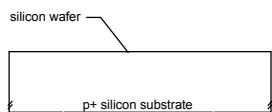


* High proportion of the total product use

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Wafer Slicing & Polishing



The silicon ingot is grown and individual wafers are sliced.

The silicon ingot is sliced into individual wafers, polished, and cleaned.

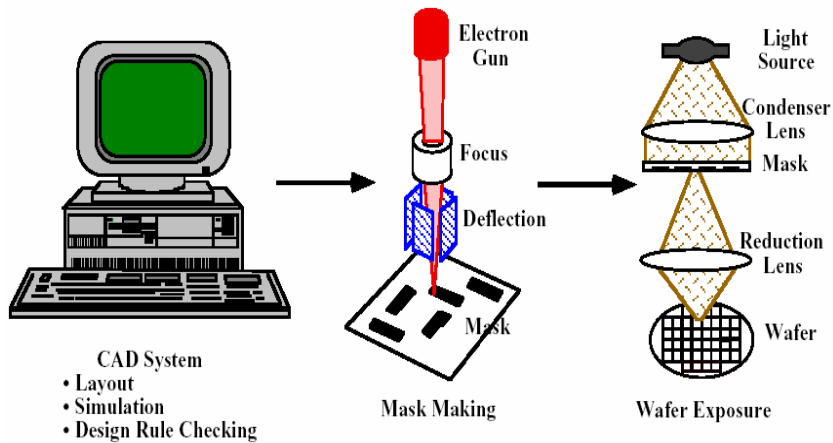
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Photolithography Concepts

- Patterning process
 - Photomask
 - Reticle
- Critical dimension generations
- Light spectrum and wavelengths
- Resolution
- Overlay accuracy
- Process latitude

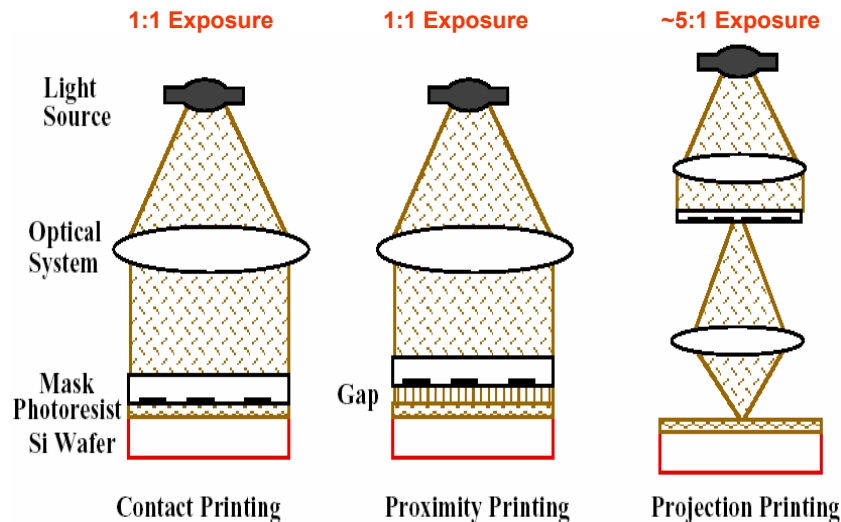
Steps in Lithography Process



Lithography has three parts:
(1) Light source, (2) Wafer exposure (3) Resist

| Year of 1st DRAM Shipment | 1997 | 1999 | 2003 | 2006 | 2009 | 2012 |
|---|-----------|-----------|--------------------|------------------|------------------|-------|
| DRAM Bits/Chip | 256M | 1G | 4G | 16G | 64G | 256G |
| Minimum Feature Size nm | | | | | | |
| Isolated Lines (MPU) | 200 | 140 | 100 | 70 | 50 | 35 |
| Dense Lines (DRAM) | 250 | 180 | 130 | 100 | 70 | 50 |
| Contacts | 280 | 200 | 140 | 110 | 80 | 60 |
| Gate CD Control 3σ (nm) | 20 | 14 | 10 | 7 | 5 | 4 |
| Alignment (mean + 3σ) (nm) | 85 | 65 | 45 | 35 | 25 | 20 |
| Depth of Focus (μm) | 0.8 | 0.7 | 0.6 | 0.5 | 0.5 | 0.5 |
| Defect Density (per layer/ m^2) | 100 | 80 | 60 | 50 | 40 | 30 |
| @ Defect Size (nm) | @ 80 | @ 60 | @ 40 | @ 30 | @ 20 | @ 15 |
| DRAM Chip Size (mm^2) | 280 | 400 | 560 | 790 | 1120 | 1580 |
| MPU Chip Size (mm^2) | 300 | 360 | 430 | 520 | 620 | 750 |
| Field Size (mm) | 22x22 | 25x32 | 25x36 | 25x40 | 25x44 | 25x52 |
| Exposure Technology | 248nm DUV | 248nm DUV | 248nm or 193nm DUV | 193nm DUV or ??? | 193nm DUV or ??? | ??? |
| Minimum Mask Count | 22 | 22/24 | 24 | 24/26 | 26/28 | 28 |

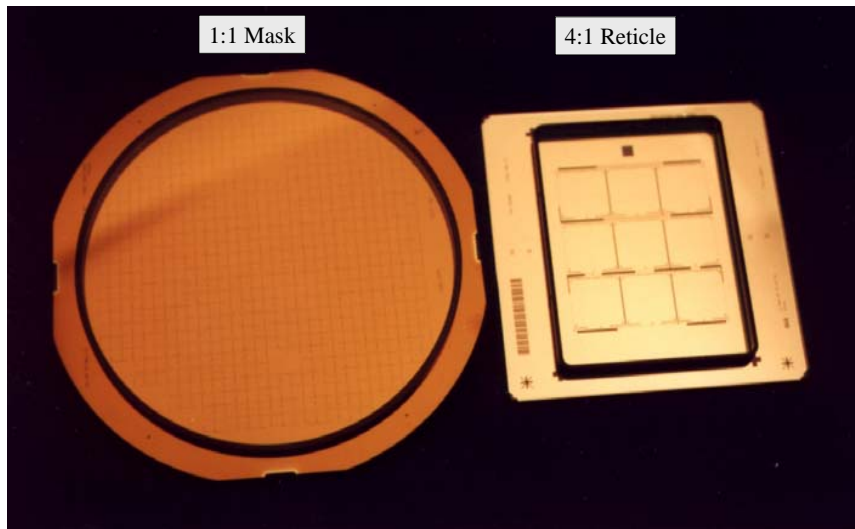
Three Basic Exposure Methods



Exposure Techniques

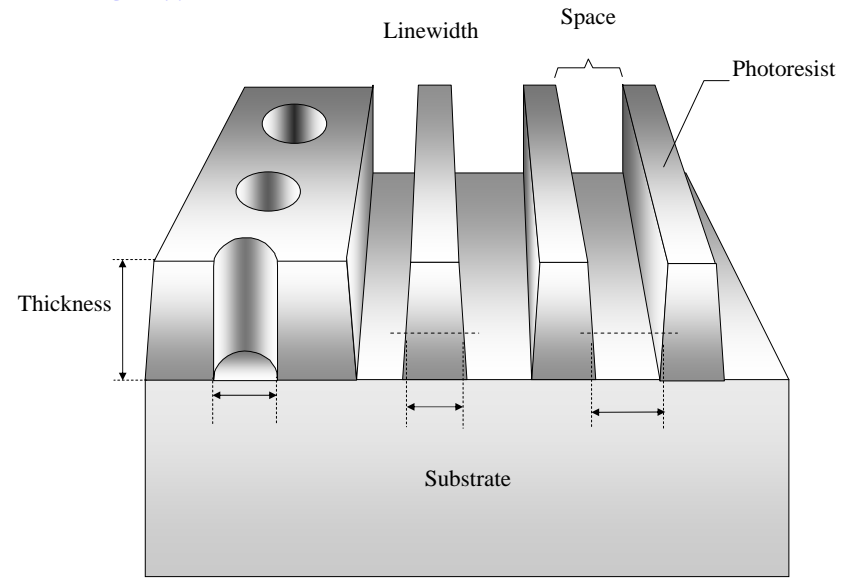
- Contact Printing
 - Simple, inexpensive, fast, limited diffraction
 - Mask wear, contamination, \$\$\$ mask
 - Resolution limited by scattering in resist
- Proximity Printing
 - No contamination
 - More diffraction
- Projection Printing
 - Tolerate more mask defects/temp variation
 - Longer to expose wafer, complex, precision stepper required

Photomask and Reticle for Microlithography



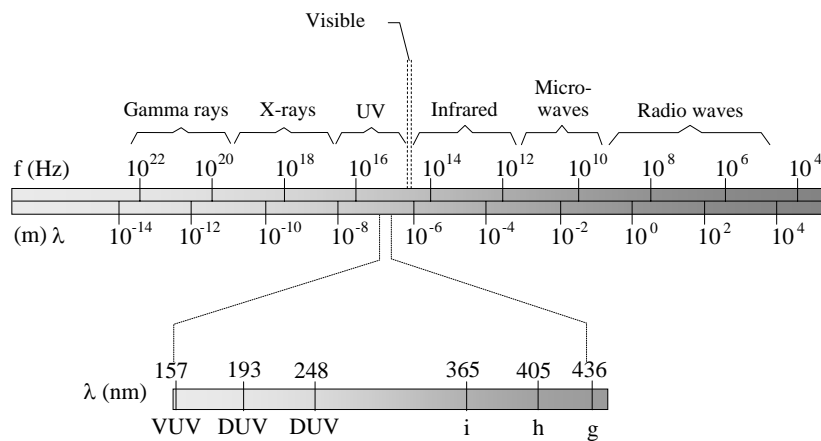
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Three Dimensional Pattern in Photoresist



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Section of the EM Spectrum



Common UV wavelengths used in optical lithography.

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Light Sources

Decreasing feature sizes requires shorter λ .

- **Hg vapor lamps:** Hg plasma inside glass lamp
 - Produces multiple wavelengths
 - Limited in intensity
 - "g" line: $\lambda = 436 \text{ nm}$ (used to mid 1980s)
 - "I" line: $\lambda = 365 \text{ nm}$ (early 1990s, $>0.3 \mu\text{m}$)
- **Deep UV by excimer lasers**
 - $\text{Kr} + \text{NF}_3 + (\text{energy}) \rightarrow \text{KrF} + (\text{photon emission})$
 - KrF: $\lambda = 248 \text{ nm}$ (used for $0.25 \mu\text{m}$)
 - ArF: $\lambda = 193 \text{ nm}$ (used for $0.12 \mu\text{m}$)

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Important Wavelengths for Photolithography Exposure

| UV Wavelength (nm) | Wavelength Name | UV Emission Source |
|--------------------|-----------------|--|
| 436 | g-line | Mercury arc lamp |
| 405 | h-line | Mercury arc lamp |
| 365 | i-line | Mercury arc lamp |
| 248 | Deep UV (DUV) | Mercury arc lamp or Krypton Fluoride (KrF) excimer laser |
| 193 | Deep UV (DUV) | Argon Fluoride (ArF) excimer laser |
| 157 | Vacuum UV (VUV) | Fluorine (F ₂) excimer laser |

13nm - EUV?

Table 13.1

Importance of Mask Overlay Accuracy

The masking layers determine the accuracy by which subsequent processes can be performed.

The photoresist mask pattern prepares individual layers for proper placement, orientation, and size of structures to be etched or implanted.

Small sizes and low tolerances do not provide much room for error.

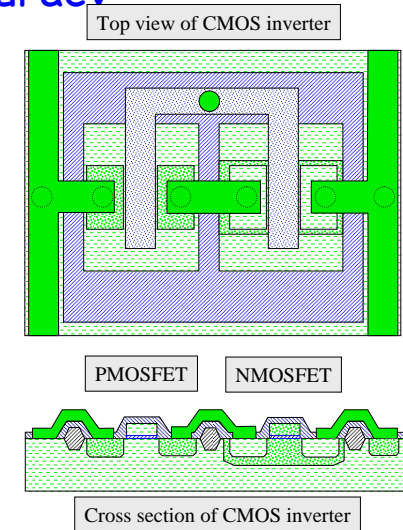
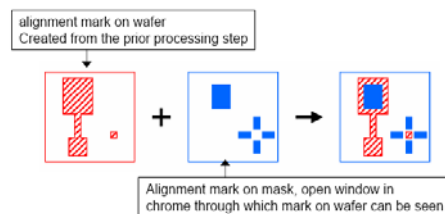


Figure 13.4

Mask/Wafer Alignment

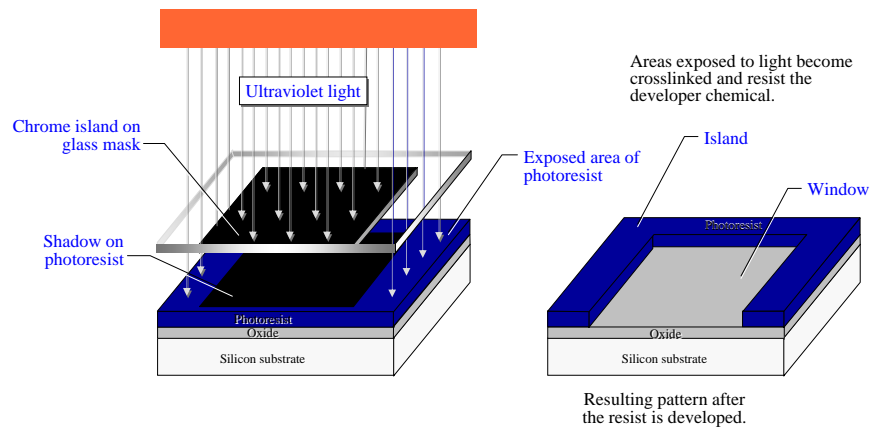
- Alignment marks on wafer (from previous pattern) and mask used to align
- Steppers do so automatically
 - Around 1-5 seconds to align
- Usually marks on left/right of stepped region



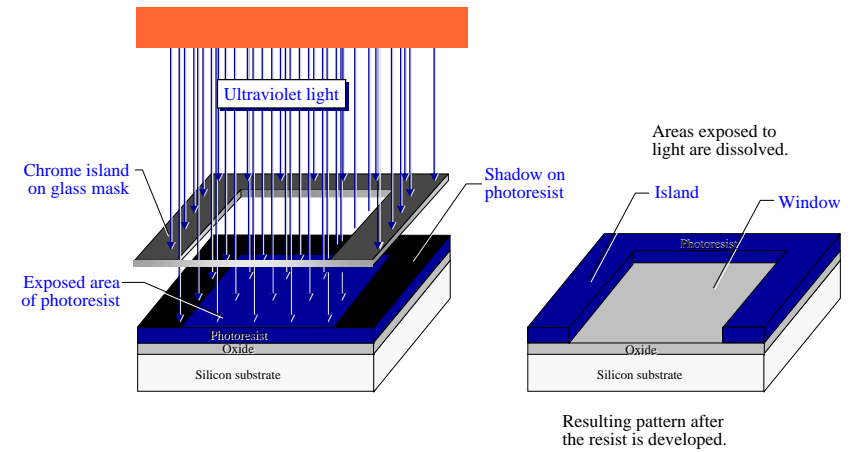
Photolithography Processes

- Negative Resist
 - Wafer image is opposite of mask image
 - Exposed resist hardens and is insoluble
 - Developer removes unexposed resist
- Positive Resist
 - Mask image is same as wafer image
 - Exposed resist softens and is soluble
 - Developer removes exposed resist

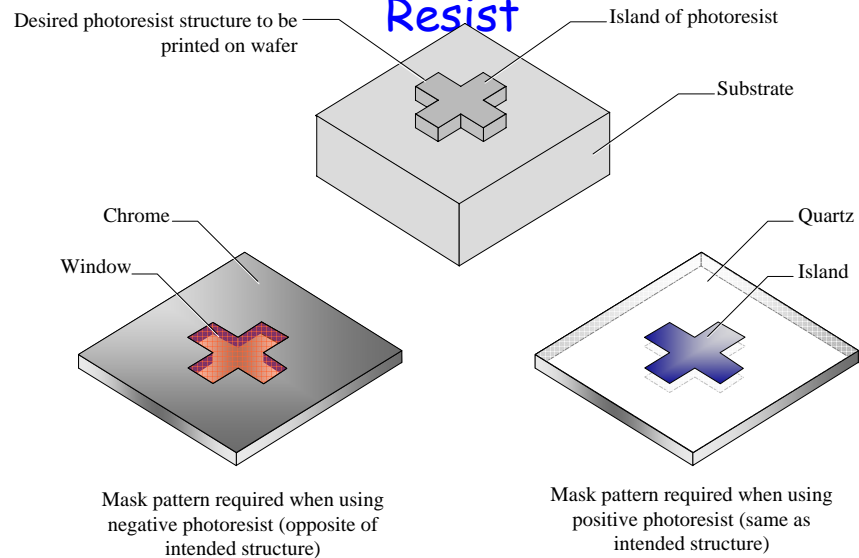
Negative Lithography



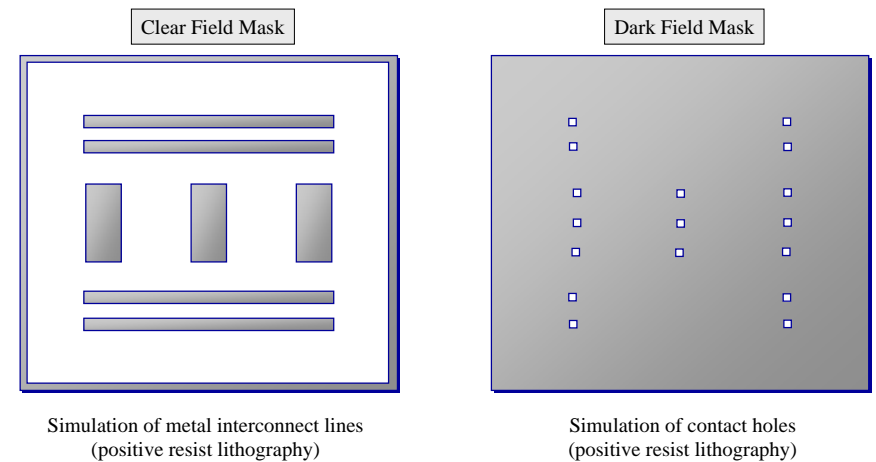
Positive Lithography



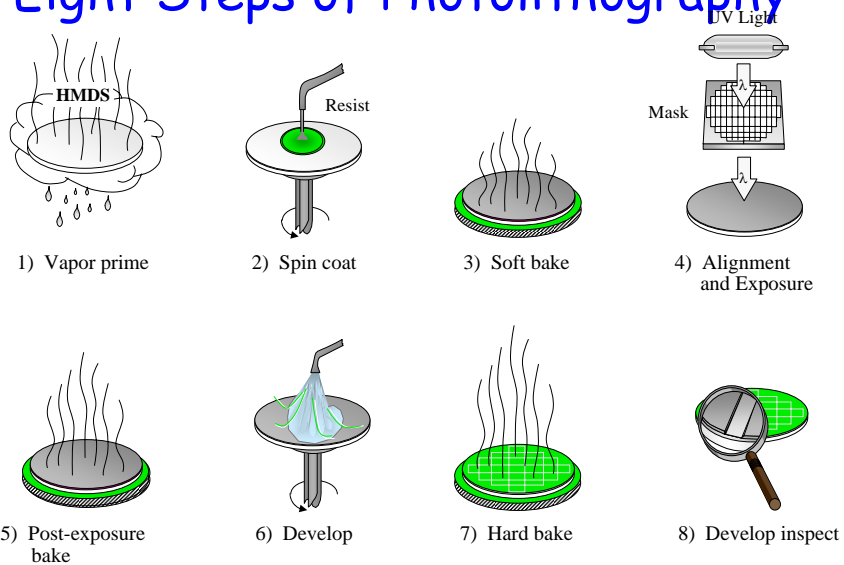
Relationship Between Mask and Resist



Clear Field and Dark Field Masks



Eight Steps of Photolithography



Photolithography Track System



Vapor Prime

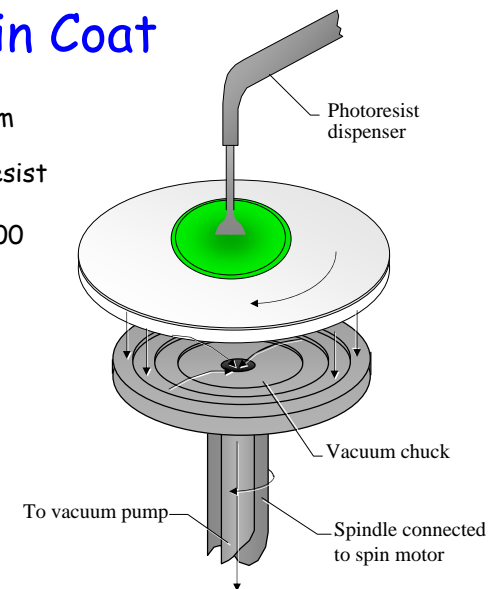
The First Step of Photolithography:

- Promotes Good Photoresist-to-Wafer Adhesion
- Primes Wafer with Hexamethyldisilazane, HMDS
- Followed by Dehydration Bake
- Ensures Wafer Surface is Clean and Dry

Spin Coat

Process Summary:

- Wafer is held onto vacuum chuck
- Dispense ~5ml of photoresist
- Slow spin ~ 500 rpm
- Ramp up to ~ 3000 to 5000 rpm
- Quality measures:
 - time
 - speed
 - thickness
 - uniformity
 - particles and defects



Soft bake

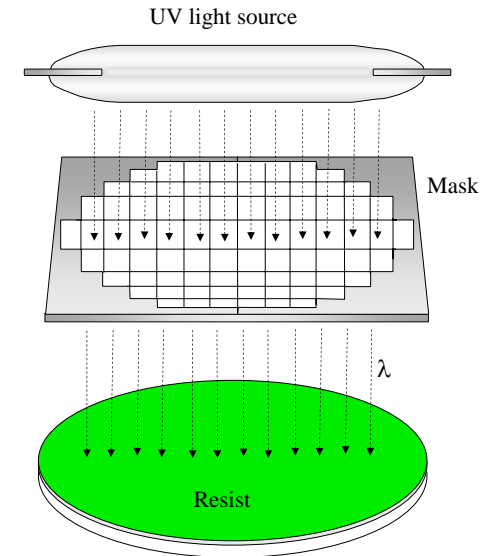
Characteristics of Soft Bake:

- Improves Photoresist-to-Wafer Adhesion
- Promotes Resist Uniformity on Wafer
- Improves Linewidth Control During Etch
- Drives Off Most of Solvent in Photoresist
- Typical Bake Temperatures are 90 to 100°C
 - For About 30 Seconds
 - On a Hot Plate
 - Followed by Cooling Step on Cold Plate

Alignment and Exposure

Process Summary:

- Transfers the mask image to the resist-coated wafer
- Activates photo-sensitive components of photoresist
- Quality measures:
 - linewidth resolution
 - overlay accuracy
 - particles and defects



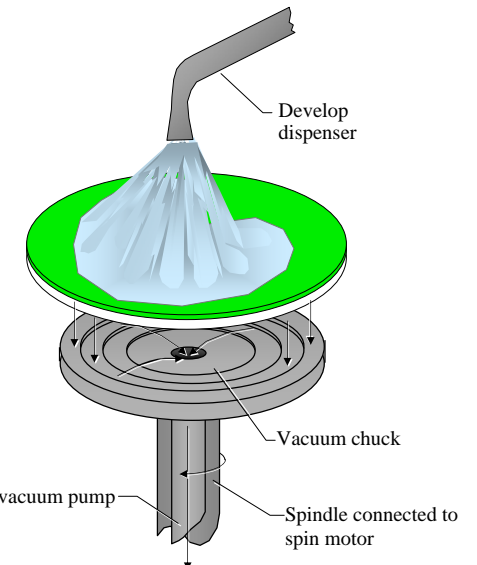
Post-Exposure Bake

- Required for Deep UV Resists
- Typical Temperatures 100 to 110°C on a hot plate
- Immediately after Exposure
- Has Become a Virtual Standard for DUV and Standard Resists

Photoresist Development

Process Summary:

- Soluble areas of photoresist are dissolved by developer chemical
- Visible patterns appear on wafer
 - windows
 - islands
- Quality measures:
 - line resolution
 - uniformity
 - particles and defects



Hard Bake

- A Post-Development Thermal Bake
- Evaporate Remaining Solvent
- Improve Resist-to-Wafer Adhesion
- Higher Temperature (120 to 140°C) than Soft Bake

Develop / Inspect

- **Inspect to Verify a Quality Pattern**
 - Identify Quality Problems (Defects)
 - Characterize the Performance of the Photolithography Process
 - Prevents Passing Defects to Other Areas
 - Etch
 - Implant
 - Rework Mis-processed or Defective Resist-coated Wafers
- Typically an Automated Operation

Purpose of Photoresist in Wafer Fab

- To transfer the mask pattern to the photoresist on the top layer of the wafer surface
- To protect the underlying material during subsequent processing e.g. etch or ion implantation.

Progressive Improvements in Photoresist

- Better image definition (resolution).
- Better adhesion to semiconductor wafer surfaces.
- Better uniformity characteristics.
- Increased process latitude (less sensitivity to process variations).

Spin Coat

- **Photoresist**
 - Types of Photoresist
 - Negative Versus Positive Photoresists
- **Photoresist Physical Properties**
- **Conventional I-Line Photoresists**
 - Negative I-Line Photoresists
 - Positive I-Line Photoresists
- **Deep UV (DUV) Photoresists**
- **Photoresist Dispensing Methods**

Types of Photoresists

- **Two Types of Photoresist**
 - Positive Resist
 - Negative Resist
- **CD Capability**
 - Conventional Resist
 - Deep UV Resist
- **Process Applications**
 - Non-critical Layers
 - Critical Layers

Negative Versus Positive Resists

- **Negative Resist**
 - Wafer image is opposite of mask image
 - Exposed resist hardens and is insoluble
 - Developer removes unexposed resist
- **Positive Resist**
 - Mask image is same as wafer image
 - Exposed resist softens and is soluble
 - Developer removes exposed resist
- **Resolution Issues**
- **Clear Field Versus Dark Field Masks**

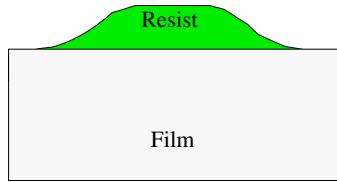
Photoresist Physical Characteristics

- ⊙ **Resolution**
- ⊙ **Contrast**
- ⊙ **Sensitivity**
- ⊙ **Viscosity**
- ⊙ **Adhesion**
- ⊙ **Etch resistance**
- ⊙ **Surface tension**
- ⊙ **Storage and handling**
- ⊙ **Contaminants and particles**

Resist Contrast

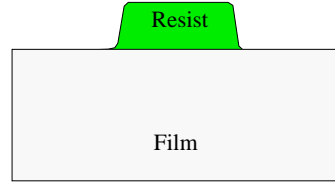
Poor Resist Contrast

- Sloped walls
- Swelling
- Poor contrast



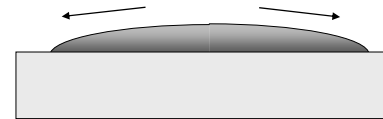
Good Resist Contrast

- Sharp walls
- No swelling
- Good contrast

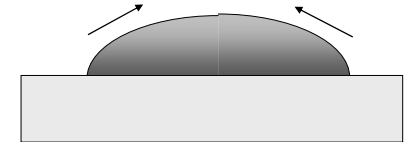


Surface Tension

Low surface tension from low molecular forces



High surface tension from high molecular forces



Components of Conventional Photoresist

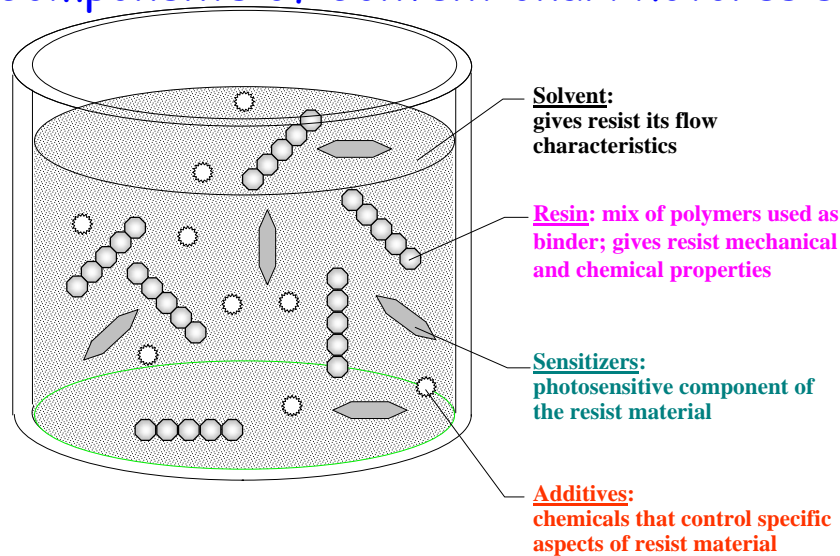
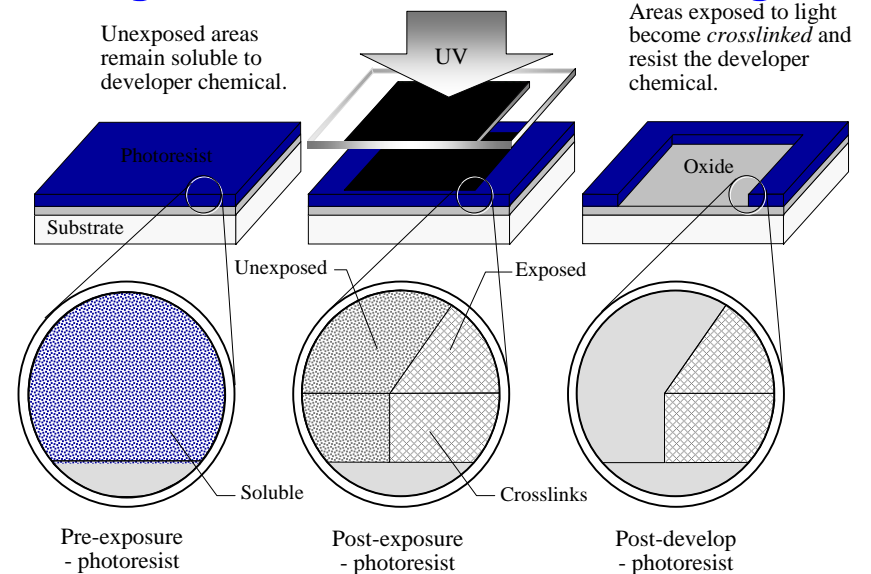


Figure 13.18

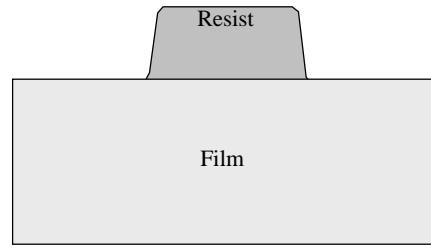
Negative Resist Cross-Linking



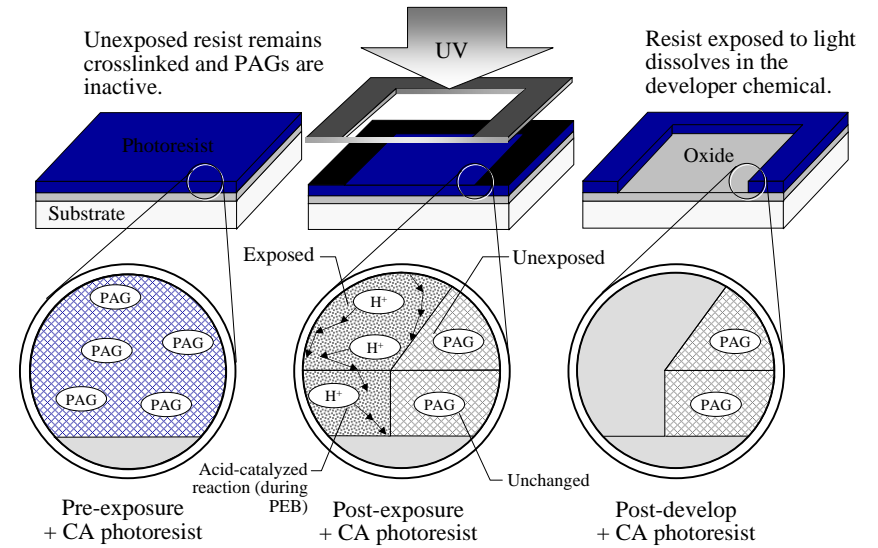
Good Contrast Characteristics of Positive I-line Photoresist

Positive Photoresist:

- Sharp walls
- No swelling
- Good contrast



Chemically Amplified (CA) DUV Resist

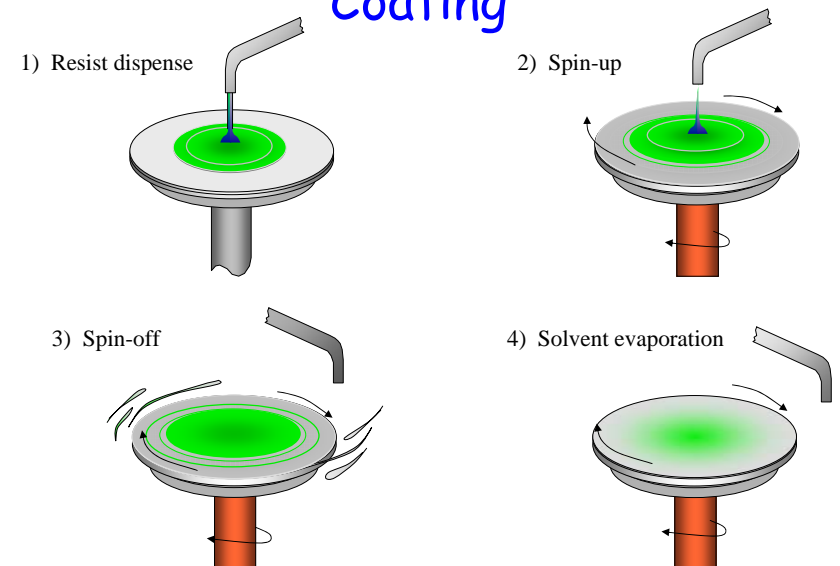


Exposure Steps for Chemically-Amplified DUV Resist

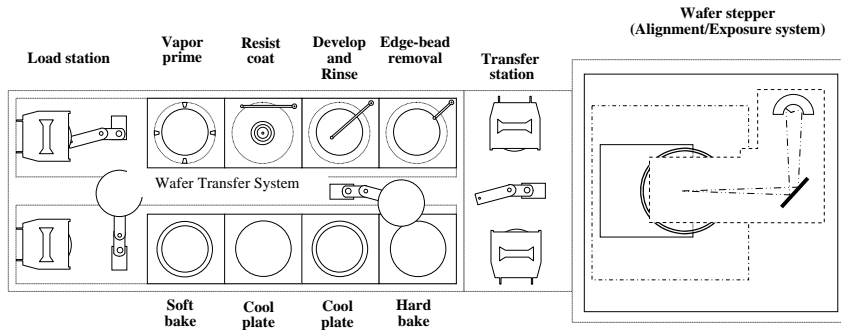
1. Resin is phenolic copolymer with protecting group that makes it insoluble in developer.
2. Photoacid generator (PAG) generates acid during exposure.
3. Acid generated in exposed resist areas serves as catalyst to remove resin-protecting group during post exposure thermal bake.
4. Exposed areas of resist without protecting group are soluble in aqueous developer.

Table 13.5

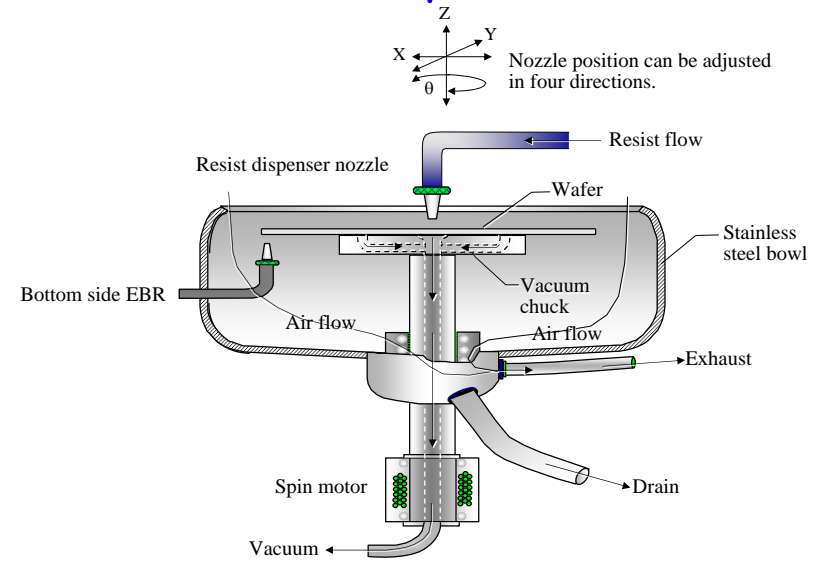
Steps of Photoresist Spin Coating



Automated Wafer Track for Photolithography



Photoresist Dispense Nozzle



Soft Bake on Vacuum Hot Plate

Purpose of Soft Bake:

- Partial evaporation of photoresist solvents
- Improves adhesion
- Improves uniformity
- Improves etch resistance
- Improves linewidth control
- Optimizes light absorbance characteristics of photoresist

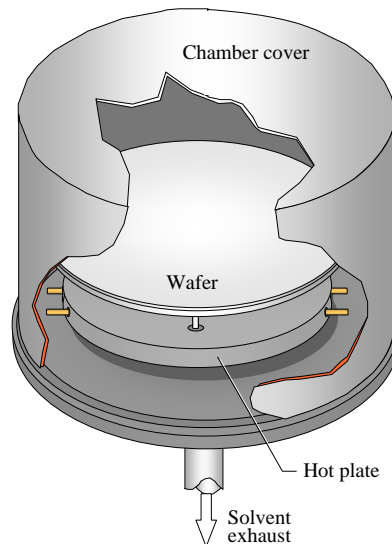


Figure 13.28

For next time

- Whiteside's article on assembly