15-398

15-398 Introduction to Nanotechnology

Nanotechnology And Computer Architecture

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Today

- · Device requirements
- Manufacturing requirements
- Fabrication
- Micro-nano scale matching
- · Reconfigurable computing
- Architectures

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Computing Devices

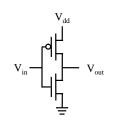
- Completeness
- Logic Restoration
- Fan-out
- Input/Output Isolation
- Power Gain
- Inexpensive
- Low power (zero static power)
- · Dense packing
- Reliable

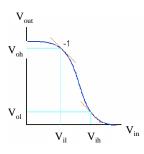
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Switching

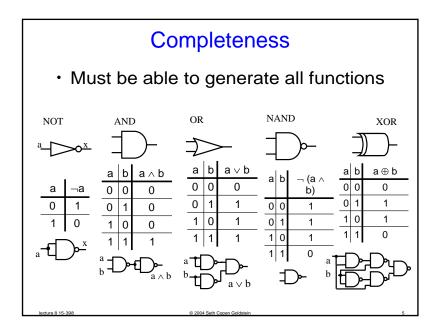
 Devices must have some non-linear characteristic that supports logical computation

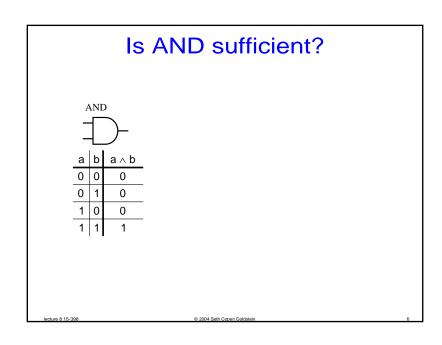


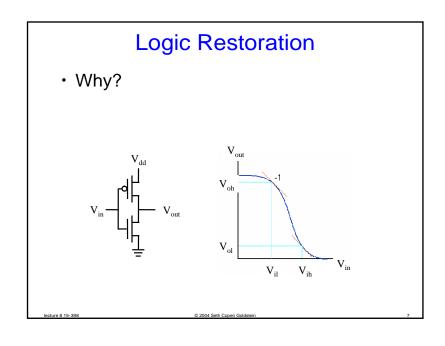


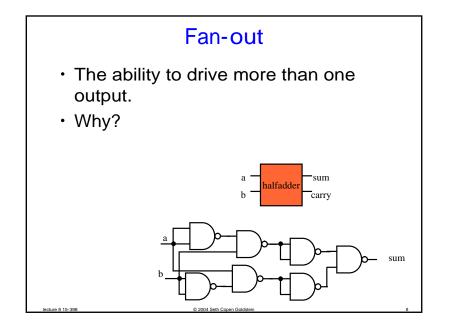
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I/O Isolation

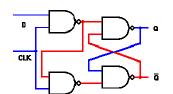
- A change in the output does not affect the value of the input.
- · Why?

Power gain

· Is it strictly necessary?

SirM model

- Switching
- Isolation
- Restoration
- Memory



Necessary Device Abstraction

- Transistor provides it all
 - Switch
 - Fan-out

 - I/O isolation
 - Signal restoration
- Necessary for

Necessary for logic

- large designs
- · Replace single abstraction with multiple abstractions: SIRM
- Enables an incremental path to direct nano-circuits

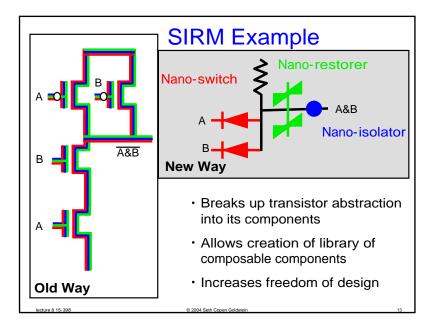
SIRM

- · SIRM decomposes the abstraction into its fundumental components.
 - Switch
 - I solation
 - Restoration
 - Memory

Necessary for logic

Necessary for large designs

- SIRM already in use
- · Allows circuit designers to explicitly manage the different components of a scalable circuit technology



Manufacturing Requirements

- Inexpensive
- Reliable
- · High yield
- Dense packing
- Scalable
- Top-Down: Photolithography-Combines manufacturing and assembly into one step!
- · Bottom-up: ?

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(scalable) Bottom-up assembly

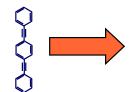
- Many different techniques:
 - Langmuir-Blodgett files
 - Flow-based alignment
 - EM alignment
 - Self-assembled monolayers
 - Chemical synthesis
 - DNA-based assembly
 - Nano-imprinting
- Separates manufacturing and assembly!
- Often, no precise placement control

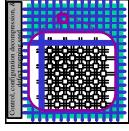
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Fabrication Is Different

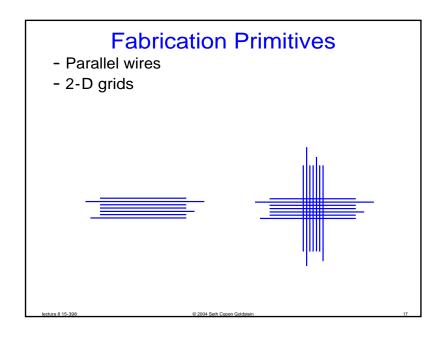
- Devices & wires alone are not useful
- Key to nanoscale computing is bottom-up assembly

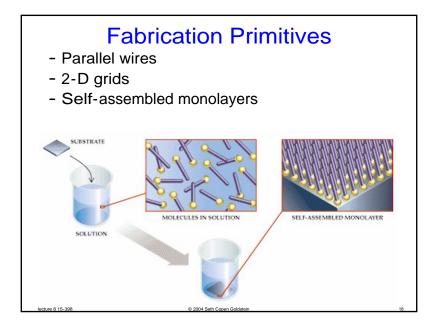


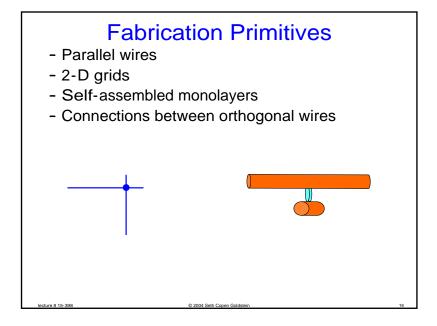


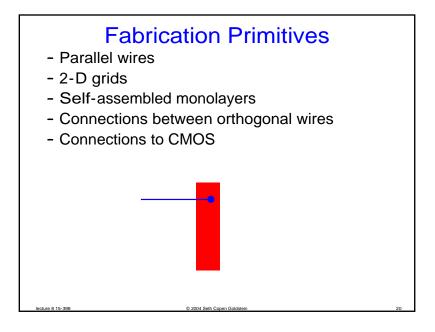
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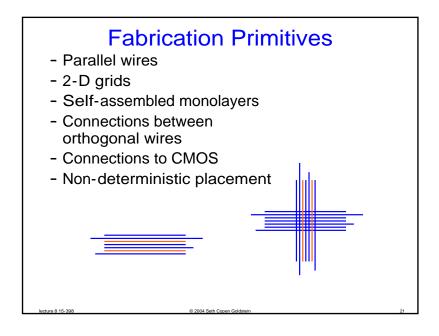
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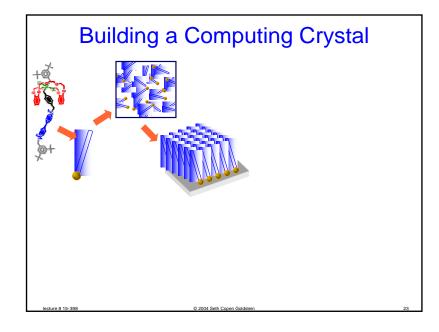


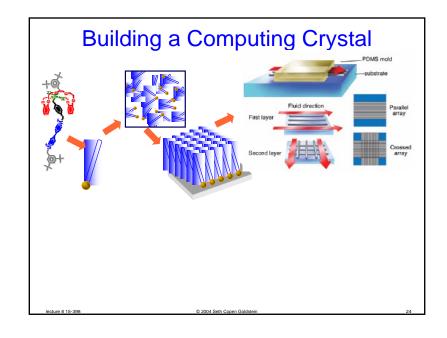
Fabrication Primitives

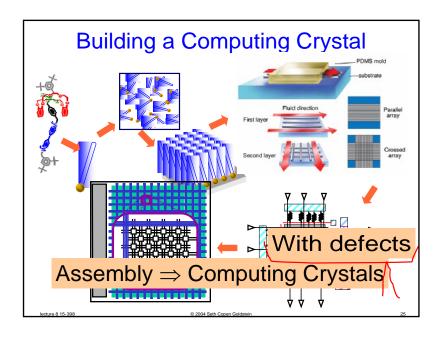
- Parallel wires
- 2-D grids
- Self-assembled monolayers
- Connections between orthogonal wires
- Connections to CMOS
- Non-deterministic placement
- Selective variability on a lithographic scale

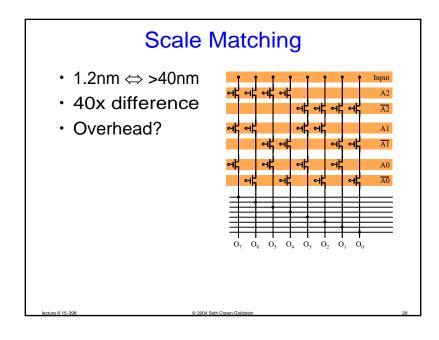


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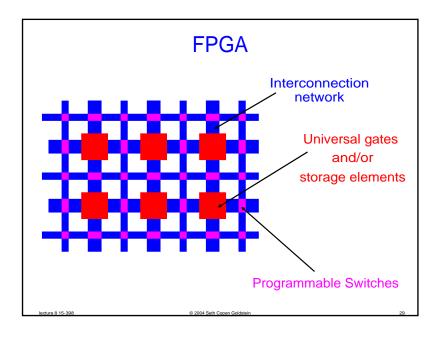
Harnessing Randomness Fab primitives prefer low information content structures Can we design circuits that can exploit this? Example: Scale Matching Address 1 nanoscale wire with 5log(N) micronscale wires Based on random placement of molecules Nanoscale wires

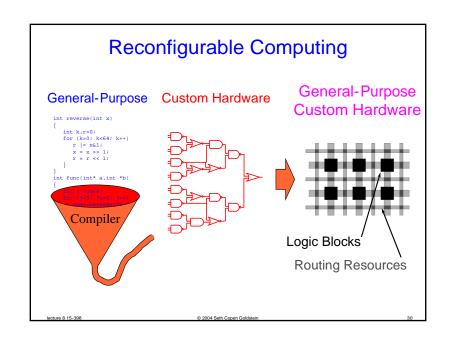
Implications

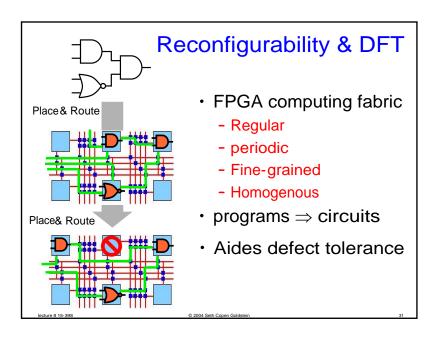
- Prefer devices at cross-points (only 2 terminal devices?)
- Only regular structures
- Defect-tolerance required
- Functionality must be added post-fabrication

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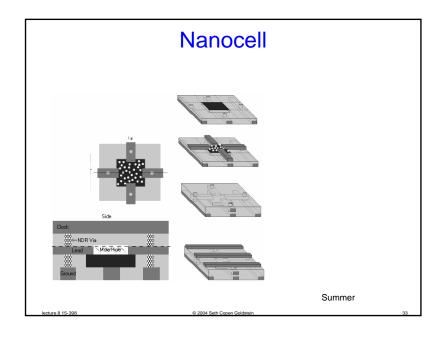


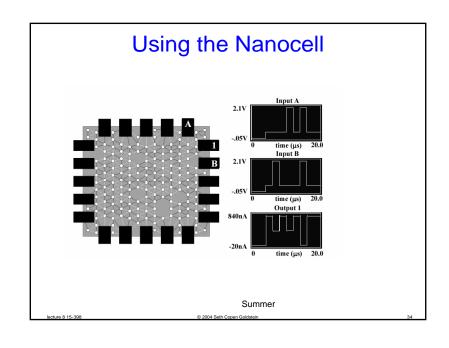


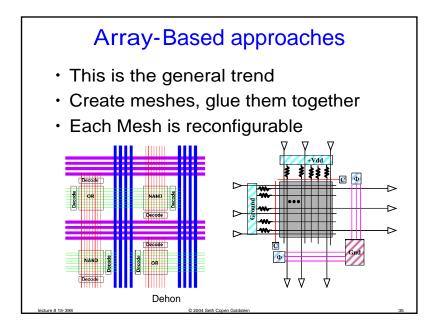
Sample Proposals

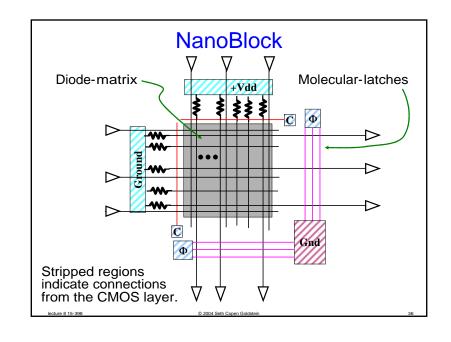
- Can be evaluated on determinism required at fab time
 - Nanocell: purely random
 - Array-based: quasi-regular
 - Nanoscale silicon: determinisitc

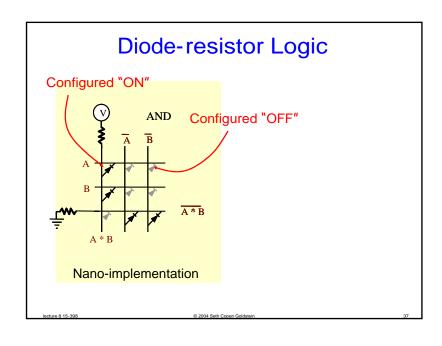
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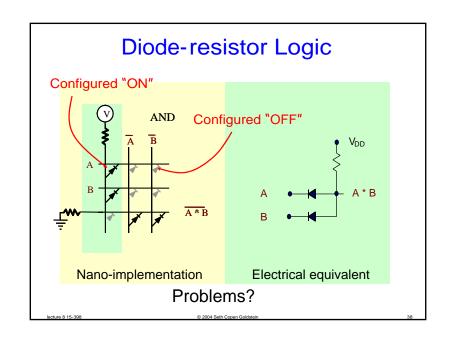


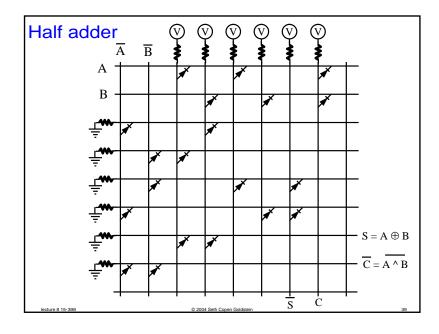


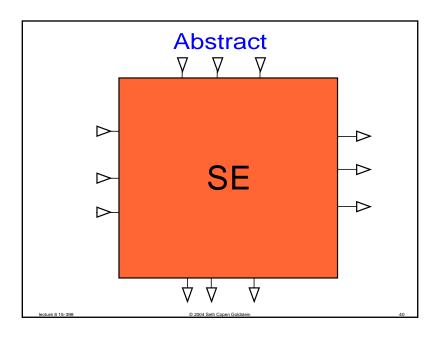


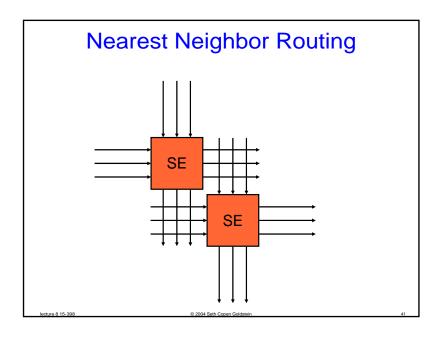


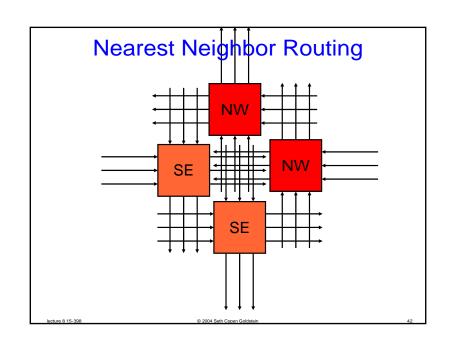


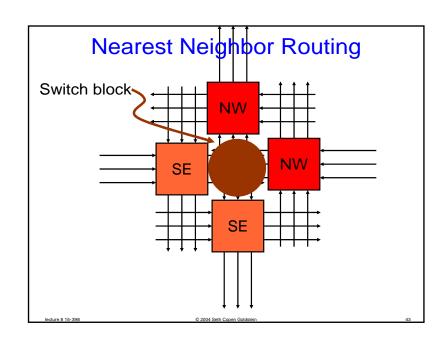


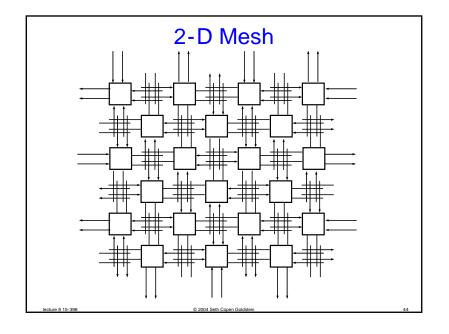


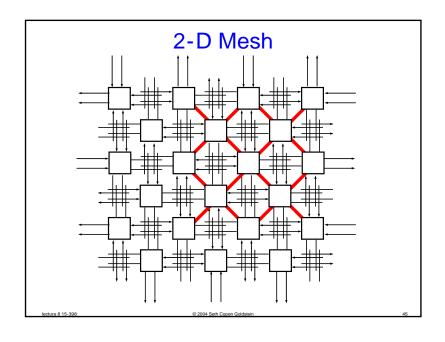


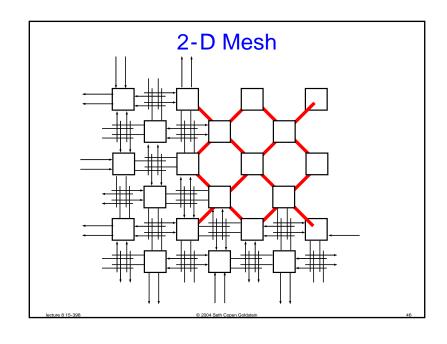


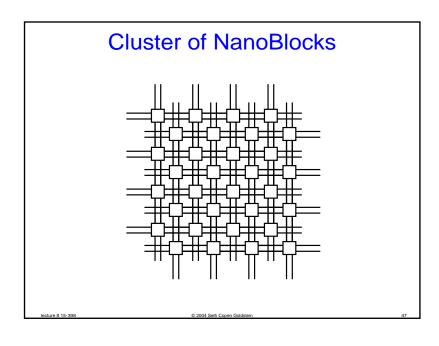


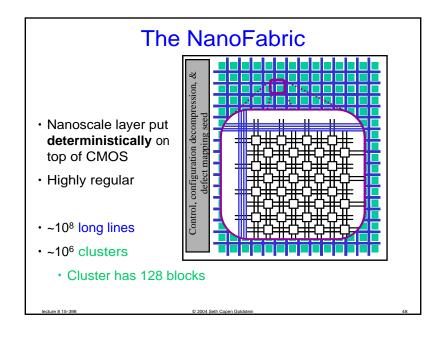












NanoFabric Attributes

- · Hierarchical fabrication
 - 1. Manufacture devices
 - 2. Non-deterministically align wires
 - 3. Self-assemble monolayers onto wires
 - 4. Create meshes
 - 5. Deterministically align w/CMOS
- Reconfigurable
- Defect tolerant

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Next Time

- Take a closer look at nano-devices
- · Read chapter 5
- · Recommended Ratner 1973

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Trade-offs

- Ease of Manufacturing Vs. ?
- · Device capabilities Vs. ?
- Device reliability Vs?
- Information content in design Vs?

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