CS 213, Spring 2000
Homework Assignment H4
Handed Out: April 6, No handin *(Practice Only)*

Prof. Mowry (`tcm@cs.cmu.edu`) is the lead person for this assignment. The purpose is to give you some practice with address translation for the exam. It will not be graded.

Problem 1

In each line of the table below, you are given a list of cache parameters: n bits of physical address, and an E-way associative cache with a line size of B bytes and a total size of D data bytes. For each list of parameters, compute the corresponding number of cache sets (S), tag bits (t), set index bits (s), and block offset bits (b).

	n	D	B	E	S	t	s	b
1.	32	1024	4	1				
2.	32	1024	4	4				
3.	32	1024	4	256				
4.	32	1024	8	1				
5.	32	1024	8	4				
6.	32	1024	8	128				
7.	32	1024	32	1				
8.	32	1024	32	4				
9.	32	1024	32	32				

Virtual Address Translation

The following problems concerns the components of the memory hierarchy and the way virtual addresses are translated into physical addresses.

- The memory is byte addressable.
- Memory accesses are to **1-byte words** (not 4-byte words).
- Virtual addresses are 14 bits wide.
- Physical addresses are 12 bits wide.
- The page size is 64 bytes.
- The TLB is 4-way set associative with 16 total entries.
- The cache is direct mapped, with a 4 byte line size and 16 total lines.

In the following tables, all numbers are given in hexadecimal. The contents of the TLB are as follows.

TLB												
Set Index	Tag	PPN	Valid	Tag	PPN	Valid	Tag	PPN	Valid	Tag	PPN	Valid
0	03	21	0	09	0D	1	00	13	0	07	02	1
1	03	2D	1	02	13	0	04	21	0	0A	11	0
2	02	00	0	08	1F	0	06	2F	0	03	11	0
3	07	29	0	03	0D	1	0A	34	1	02	1B	0

The page table for the first 16 pages and the cache are as follows:

Page Table					
VPN	PPN	Valid	VPN	PPN	Valid
000	28	1	008	13	1
001	2B	0	009	17	1
002	33	1	00A	09	1
003	02	1	00B	1A	0
004	2A	0	00C	27	0
005	16	1	00D	2D	1
006	04	0	00E	11	1
007	26	0	00F	0D	1

Cache						
Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	19	1	99	11	23	11
1	15	0	55	59	0B	41
2	1B	1	00	02	04	08
3	36	0	84	06	B2	9C
4	32	1	43	6D	8F	09
5	0D	1	36	72	F0	1D
6	31	0	A2	37	68	10
7	16	1	11	C2	DF	03
8	24	1	3A	00	51	89
9	2D	0	46	92	88	FE
A	2D	1	93	15	DA	3B
B	0B	0	71	49	10	05
C	12	0	82	03	02	12
D	16	1	04	96	34	15
E	13	1	83	77	1B	D3
F	14	0	20	07	12	19

Problem 2

A. The box below shows the format of a virtual address. Indicate (by labeling the diagram) the fields that would be used to determine the following:

VPO The virtual page offset
VPN The virtual page number
TLBI The TLB index
TLBT The TLB tag

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. The box below shows the format of a physical address. Indicate (by labeling the diagram) the fields that would be used to determine the following:

PPO The physical page offset
PPN The physical page number
CO The byte offset within the cache line
CI The cache index
CT The cache tag

11	10	9	8	7	6	5	4	3	2	1	0

For the following problems, you are to show how the memory system translates a virtual address into a physical address and accesses the cache.

For the given virtual address, indicate the TLB entry accessed, the physical address, and the cache byte value returned. Indicate whether the TLB misses, whether a page fault occurs, and whether a cache miss occurs.

If there is a cache miss, enter "-" for "Cache Byte returned". If there is a page fault, enter "-" for "PPN" and leave parts C and D blank.

Problem 3

Virtual address: `027C`

A. Virtual address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

Problem 4

Virtual address: `03D4`

A. Virtual address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

Problem 5

Virtual address: `03A9`

A. Virtual address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

Problem 6

Virtual address: `03D7`

A. Virtual address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

Problem 7

Virtual address: `0040`

A. Virtual address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

SOLUTIONS

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Problem 1

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S = D/(BE)
t = n - s - b
s = log2(s)
b = log2(b)

n	D	B	E	S	t	s	b
32	1024	4	1	256	22	8	2
32	1024	4	4	64	24	6	2
32	1024	4	256	1	30	0	2
32	1024	8	1	128	22	7	3
32	1024	8	4	32	24	5	3
32	1024	8	128	1	29	0	3
32	1024	32	1	32	22	5	5
32	1024	32	4	8	24	3	5
32	1024	32	32	1	27	0	5

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Problem 2

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A. VPN: [13-6] VPO: [5-0]
TLBT: [13-8] TLBI: [7-6]

B. PPN: [11-6] PPO: [5-0]
CT: [11-6] CI: [5-2] CO: [1-0]

```
*********
Problem 3
*********
 A. 00 0010 0111 1100

 B.     VPN:            0x9
        TLBI:           0x1
        TLBT:           0x2
        TLB hit?        N
        page fault?     N
        PPN:            0x17

 C.     0101 1111 1100

 D.     CO:             0x0
        CI:             0xf
        CT:             0x17
        cache hit?      N
        cache byte?     -

*********
Problem 4
*********
 A. 00 0011 1101 0100

 B.     VPN:            0xf
        TLBI:           0x3
        TLBT:           0x3
        TLB hit?        Y
        page fault?     N
        PPN:            0xd

 C.     0011 0101 0100

 D.     CO:             0x0
        CI:             0x5
        CT:             0xd
        cache hit?      Y
        cache byte?     0x36
```

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*********
Problem 5
*********
 A. 00 0011 1010 1001

 B.      VPN:             0xe
         TLBI:            0x2
         TLBT:            0x3
         TLB hit?         N
         page fault?      N
         PPN:             0x11

 C.      0100 0110 1001

 D.      CO:              0x1
         CI:              0xa
         CT:              0x11
         cache hit?       N
         cache byte?      -

*********
Problem 6
*********
 A. 00 0011 1101 0111

 B.      VPN:             0xf
         TLBI:            0x3
         TLBT:            0x3
         TLB hit?         Y
         page fault?      N
         PPN:             0xd

 C.      0011 0101 0111

 D.      CO:              0x3
         CI:              0x5
         CT:              0xd
         cache hit?       Y
         cache byte?      0x1d
```

```
*********
Problem 7
*********
 A. 00 0000 0100 0000

 B.      VPN:             0x1
         TLBI:            0x1
         TLBT:            0x0
         TLB hit?         N
         page fault?      Y
         PPN:             -

 C.      n/a

 D.      n/a
```