Automatic Verification of Asynchronous Circuits

by

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Abstract.

Establishing the correctness of complicated asynchronous circuit is in general quite difficult because of the high degree of nondeterminism that is inherent in such devices. Nevertheless, it is also very important in view of the cost involved in design and testing of circuits. We show how to give specifications for circuits in a branching time temporal logic and how to mechanically verify them using a simple and efficient model checker. We also show how to tackle a large and complex circuit by verifying it hierarchically.

0. Introduction.

Verification of the correctness of asynchronous circuits has been considered an important problem for a long time. But, a lack of any formal and efficient method of verification has prevented the creation of practical design aids for this purpose. Since all the known techniques of simulation and prototype testing are time-consuming and not very reliable, there is an acute need for such tools. Moreover, as we build larger and more complex circuits, the cost of a single design error is likely to become even higher. In this paper, we describe an automatic verification system for asynchronous circuits, in which the specifications are expressed in a propositional temporal logic. We illustrate the use of our system by verifying a version of the self-timed queue element given in [MC80].

Bochmann [BO82] was probably the first to recognize the usefulness of temporal logic to describe circuits; he verified an implementation of a self-timed arbiter using linear temporal logic and what he called “reachability analysis”. The work of Malchi and Owicki [MO82] identified additional temporal operators required to express interesting properties of a circuit and also gave specifications of a large class of modules used in self-timed systems.

Although these researchers have contributed significantly toward developing an adequate notation for expressing the correctness of asynchronous circuits, the problem of mechanically verifying a circuit using efficient algorithms still remains unsolved. In this paper we show how a simple and efficient algorithm, called a model checker, can be used to verify various temporal properties of an asynchronous circuit. Roughly speaking, our method works by first building a labelled state-transition graph for an asynchronous circuit. This graph can be viewed as a finite Kripke Structure. Then by using the model checker we determine the truth of various temporal formulae in this Kripke Structure. As a result, it is possible to avoid the complexity associated with proof construction.

Most complex circuits are built out of relatively less complex modules in a hierarchical manner. Hence it should be possible to verify these circuits in a hierarchical manner, i.e. to verify the correctness of a larger module, given the premises that the smaller modules are correct. A hierarchical approach to verification is important in practice, because it enables us to verify circuits incrementally, to localize faults to small submodules and most importantly, to handle large circuits without a large growth in complexity. We show how the hierarchical method can be incorporated in a mechanical approach to circuit verification.

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The paper is organized as follows: Section 1 contains a brief description of the syntax and semantics of CTL, the temporal logic used in this paper, and also explains the algorithms used in the model checker. In Section 2, we give a simple step-by-step method used to verify circuits. In Section 3, we illustrate these methods by establishing some interesting properties of a Self-Timed Queue (FIFO) Element. In Section 4, we introduce a hierarchical method to be used in verifying large and complex circuit and study some of the model-theoretic properties of the operation of "restriction" on a Kripke Structure. The paper concludes by pointing out the shortcomings of our approach and with a discussion of some remaining open problems.

1. CTL and Model Checker.

The logic that we use to give the specifications of a circuit is a propositional temporal logic of branching time, called CTL (Computation Tree Logic). This logic is essentially the same as that described in [CES83], [EC80] and [BMP81].

The syntax for CTL is given below:

Let \( \mathcal{P} \) be the set of all the atomic propositions in the language, \( \mathcal{L} \). Then

1. Every atomic proposition \( P \) in \( \mathcal{P} \) is a formula in CTL.
2. If \( f_1 \) and \( f_2 \) are CTL formul\( \text{a} \), then so are \( -f_1 \), \( f_1 \land f_2 \), \( \forall X f_1 \), \( \exists X f_1 \), \( \forall [f_1 \cup f_2] \) and \( \exists [f_1 \cup f_2] \).

In this logic the propositional connectives \( - \) and \( \land \) have their usual meanings of negation and conjunction. The temporal operator \( X \) is the nexttime operator. Hence the intuitive meaning of \( \forall X f_1 \) (\( \exists X f_1 \)) is that \( f_1 \) holds in every (in some) immediate successor state of the current state. The temporal operator \( U \) is the until operator. The intuitive meaning of \( \forall [f_1 \cup f_2] \) (\( \exists [f_1 \cup f_2] \)) is that for every computation path (for some computation path), there exists an initial prefix of the path such that \( f_2 \) holds at the last state of the prefix and \( f_1 \) holds at all other states along the prefix.

We also use the following syntactic abbreviations:

\[ f_1 \lor f_2 \equiv -(-f_1 \land -f_2) \]
\[ f_1 \rightarrow f_2 \equiv -f_1 \lor f_2 \]
\[ f_1 \leftrightarrow f_2 \equiv (f_1 \rightarrow f_2) \land (f_2 \rightarrow f_1) \]
\[ \forall F f_1 \equiv \forall [\text{true} \cup f_1] \] which means for every path, there exists a state on the path at which \( f_1 \) holds.
\[ \exists F f_1 \equiv \exists [\text{true} \cup f_1] \] which means for some path, there exists a state on the path at which \( f_1 \) holds.
\[ \forall G f_1 \equiv \neg \exists F \neg f_1 \] which means for every path, at every node on the path \( f_1 \) holds.
\[ \exists G f_1 \equiv \neg \forall F \neg f_1 \] which means for some path, at every node on the path \( f_1 \) holds.
\[ \forall [f_1 \mathbf{W} f_2] \equiv -\exists [(f_1 \land f_2) \cup (\neg f_1 \land f_2)] \] which means that for every computation path, and for every initial prefix of the path, if \( f_2 \) holds at all the states along the prefix then \( f_1 \) holds at all the states along the same prefix.
\[ \exists [f_1 \mathbf{W} f_2] \equiv -\forall [(f_1 \land f_2) \cup (\neg f_1 \land f_2)] \] which means that for some computation path, and for every initial prefix of the path, if \( f_2 \) holds at all the states along the prefix then \( f_1 \) holds at all the states along the same prefix.

In the last two formul\( \text{a} \) \( W \) is the \textit{while} operator. The formula \( \forall [f_1 \mathbf{W} f_2] \) (\( \exists [f_1 \mathbf{W} f_2] \)) is read as "for every (some) path \( f_1 \text{ while } f_2 \)"
The semantics of a CTL formula is defined with respect to a labelled state-transition graph. A CTL structure is a triple $(M, R, H)$ where

1. $S$ is a finite set of states.
2. $R$ is a total binary relation on $S (R \subseteq S \times S)$ and denotes the possible transitions between states.
3. $H$ is an assignment of atomic propositions to states, i.e. $H : 2^S \rightarrow 2^p$.

A path is an infinite sequence of states $(s_0, s_1, s_2, \ldots)$ such that $\forall i[(s_i, s_{i+1}) \in R]$. For any structure $M = (S, R, H)$ and state $s_0 \in S$, there is an infinite computation tree with root labelled $s_0$ such that $s \rightarrow t$ is an arc in the tree iff $(s, t) \in R$.

The truth in a structure is expressed by $s_0 \models f$, meaning that the temporal formula $f$ is satisfied in the structure $M$ at state $s_0$. The semantics of temporal formulae is defined inductively as follows:

- $s_0 \models P$ iff $P \in H(s_0)$.
- $s_0 \models \neg f$ iff $s_0 \not\models f$.
- $s_0 \models f_1 \land f_2$ iff $s_0 \models f_1$ and $s_0 \models f_2$.
- $s_0 \models \forall X f_1$ iff for all states $t$ such that $(s_0, t) \in R, t \models f_1$.
- $s_0 \models \exists X f_1$ iff for some state $t$ such that $(s_0, t) \in R, t \models f_1$.
- $s_0 \models [f_1 \lor f_2]$ iff for all paths $(s_0, s_1, s_2, \ldots), \exists i \geq 0[s_i \models f_2 \land \forall l \leq i[s_i \models f_1]]$.
- $s_0 \models \exists[f_1 \lor f_2]$ iff for some path $(s_0, s_1, s_2, \ldots), \exists i \geq 0[s_i \models f_2 \land \forall l \leq i[s_i \models f_1]]$.

From these it is quite easy to see that the semantics of $U$, the until operator can be easily given in terms of a least fixed-point characterization:

- $\forall[f_1 U f_2] \equiv \mu f_3[f_1 \land \forall X f_3].$
- $\exists[f_1 U f_2] \equiv \mu f_3[f_1 \land \exists X f_3].$

The Model Checker for CTL can now be thought of as an algorithm that determines the satisfiability of a given temporal formula $f_1$ in a model $M$, by computing these fixed points. A full description of the algorithm is given in [CES83].

In order to determine if a CTL formula $f$ is true in a structure $M = (S, R, H)$, the algorithm labels each state of $S$ so that when the algorithm terminates, the label of each state $s \in S$, $\text{label}(s)$, will be equal to $\{f' \in \text{sub}(f) \mid M, s \models f', \}$, where each element of $\text{sub}(f)$ is either a subformula of $f$ or the negation of the subformula. Hence $M, s \models f$ iff $f \in \text{label}(s)$ at the termination of the algorithm.

The labelling algorithm works in several stages. In the $i^{th}$ stage the algorithm labels the states by the subformula of length $i$. The labels assigned in the earlier stages, corresponding to the subformulas of length less than $i$, are used to perform the labelling in this stage. It can be shown that the algorithm makes at most $n = |f|$ stages of computation and that the total amount of the work involved in each stage is $O(||S|| + ||R||)$. Hence the time complexity of the Model Checker is $O(|f| \cdot (||S|| + ||R||))$. The algorithm is also fairly simple, since it involves only a few straightforward graph-theoretic algorithms.
2. Verification of Circuits.

Given a circuit to be verified, the steps involved in using the Model Checker to assert the correctness of the temporal specifications are as follows:

Step 1. Building the Model.

The structure associated with the circuit is essentially a finite state-transition graph, with its vertices corresponding to the distinct states and the edges corresponding to the (possibly nondeterministic) transition between the states. The initial label associated with each state is the set of propositions true in that state. This labelled state-transition graph can be built using the following simple algorithm:

begin
    L := {initial state};
    while L ≠ ∅ do
        choose a state, say s from L, and delete it from L;
        for all sets of inputs, possible in s do
            simulate s with this set of inputs;
            let L′ be the set of new states;
            for each s′ ∈ L′ do
                s′ is a successor of s;
                if s′ has not been visited then
                    add s′ to L;
            end;
        end;
    end;
end.

Algorithm 2.1
The Algorithm to build the Kripke Structure for an Asynchronous Circuit.

Step 2. Giving the Specifications of the Circuit in CTL.

This corresponds to the specifications of the temporal behaviour of the circuit. It usually involves structural properties (i.e. the specifications for different components of the circuit, specifications of the signalling scheme used for communication with various other modules, etc.), safety properties and liveness properties. It should probably be pointed out that one need not give the complete specification of the circuit in order to verify some selected properties of the circuit using the model checker.

Step 3. Verifying the Circuit using the Model Checker.

This step involves the model checker which checks the truth of the specification (a formula in CTL) in the structure constructed in the step 1. The working of the Model Checker is described in the previous section.
3. Extended Example.

We illustrate the ideas presented so far by verifying some interesting properties of an asynchronous circuit. The example chosen for this purpose is one element of a Self-timed (FIFO) Queue, which originally appeared in an article by C. Seitz on self-timed system [MC80].

![Figure 3.1. Queue (FIFO) element](image)

**Figure. 3.1.**

Queue (FIFO) element

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**a. Self-Timed FIFO Queue Element:** The electrical circuit shown in figure 3.1 is an implementation of a single FIFO queue element combined with some input and output logic. This circuit is of very practical importance; in pipeline processes in which operation times are variable, increased throughput can be achieved by interconnecting the processing elements through queues. The implementation uses simple asynchronous control and hence, can be used to build very fast and area-efficient queues.

The *inner cell* is intended to be replicated as many times as the number of words the queue is to be able to store, and the same control will operate a queue of any word length. The *input cell* and the *output cell* can be thought of as logic circuits converting the two-cycle signalling scheme at the input link to a four-cycle signalling scheme at the internal link and *vice versa*. The *inner cell* can be thought of as a latch that stores the state of the cell (*i.e.* whether the cell is *full* or *empty*), together with logic to generate a *load* signal and a set of *static registers* to store the *bits*. However, the design shown is not speed-independent, and uses the 3/2-rules. That is one may expect misoperation if particular sets of 3 gates have a smaller cumulative propagation delay time than other sets of 2 gates.

In the following subsections we specify and verify some interesting properties of the Queue element with a single inner cell.
b. **Temporal Specifications for the Self-Timed Queue Element**: We give examples of the ways in which various properties of a circuit can be given in CTL. In case of the Queue Element some of the structural properties that we might like to specify, are that the two-cycle signalling used at the input links and the output links is safe and live. Recall that the structural properties are specifications for various components and signalling schemes and thus, may be considered as premises that must be true in any CTL structure modelling the circuit. Hence the request signal must satisfy the following safeness and liveness conditions. (In the following CTL specifications we will use symbols Req and Ack for the request and the acknowledgement signals respectively.)

**Safeness Conditions for the Request Signal.**

1. $\forall G((\neg Req \land Ack) \rightarrow \forall F(\neg Req))$
2. $\forall G(( Req \land \neg Ack) \rightarrow \forall F(Req))$

These two CTL formulae essentially express that if the Req and Ack signals are non-equipotential then the Req signal will remain in its stable logic value while Ack signal is in its stable value. In other words, Req will not be given unless acknowledgement to previous request signal has arrived.

**Liveness Conditions for the Request Signal.**

1. $\forall G(( Req \land Ack) \rightarrow \forall F(Req))$
2. $\forall G((\neg Req \land \neg Ack) \rightarrow \forall F(Req))$

These two CTL formulae express the property that if the Req and Ack signals are equipotential then eventually the Req signal will change its logic value, thus indicating an arrival of a request.

In a similar manner, we can specify the properties of the response signal.

**Safeness Conditions for the Response Signal.**

1. $\forall G(( Req \land Ack) \rightarrow \forall F(Ack))$
2. $\forall G((\neg Req \land \neg Ack) \rightarrow \forall F(Req))$

Informally, they express the fact that Ack will not be given unless there has been a Req signal to cause it.

**Liveness Conditions for the Response Signal.**

1. $\forall G(( Req \land \neg Ack) \rightarrow \forall F(Ack))$
2. $\forall G((\neg Req \land Ack) \rightarrow \forall F(\neg Ack))$

That is, if there had been a Req signal then eventually there will be an Ack signal in response to the request.

We can also give the safeness and the liveness properties of the FIFO Queue element in CTL. The following is a representative list of some of the properties, and by no means, exhaustive and complete. In the CTL formulæ given below, ReqIn stands for request at the input links, AckIn, for acknowledgement at the input links, ReqOut, for request at the output links, AckOut, for acknowledgement at the output links and Full1, for the state of the queue element when it holds some data.
Some Safeness Properties of the Queue Element.

1. $\forall G(\neg (\text{ReqIn}=\text{AckIn}) \land \neg (\text{ReqOut}=\text{AckOut}) \rightarrow \forall [\neg (\text{ReqIn}=\text{AckIn}) \cup (\text{ReqOut}=\text{AckOut})])$

This formula states that if there have been a ReqIn and a ReqOut, then AckIn will not be given until AckOut has arrived.

Some Liveness Properties of the Queue Element.

1. $\forall G(\neg (\text{ReqIn}=\text{AckIn}) \land \neg \text{Full0} \rightarrow \forall F(A))$

This formula states that if there has been a ReqIn, and the memory element was empty, then eventually it will be loaded with the input data.

2. $\forall G(\text{Full1} \rightarrow \forall F(\neg (\text{ReqOut}=\text{AckOut})))$

That is the Queue Element is full then eventually a request at the output links will be generated in order to move the data to the next element in the queue.

3. $\forall G((\text{ReqOut}=\text{AckOut}) \rightarrow \forall F(\neg \text{Full1}))$

That is if the acknowledgement arrives at the output links thus indicating that the data stored in the current Queue Element has been moved to the next element, then eventually the Queue Element will mark its state as empty.

In the next subsection we show how these specifications can be verified automatically by using a Model Checker.

c. Verification of the Circuit: As a first step for the verification of the circuit, we build a labelled finite state-transition graph corresponding to the circuit given in figure 3.1, using the algorithm given in section 2. For this model, we assume that each gate of the circuit has one unit delay. This is done in order to take care of the speed-dependent properties of the circuit. This is equivalent to assuming that for any state in the graph, any of the successor states is arrived at after one unit gate-delay. The label associated with each state is the set of nodes in the circuit which assume the logical value 1 in that state. The initial state corresponds to the situation when ReqIn and AckIn as well as ReqOut and AckOut are equipotential.

Now, the model checker can take a description of the model and a temporal formula specifying some property of the circuit, and determine truth of the formula in that model. However the circuit shown does not obey the 3/2 rule as advertised, and the model checker determines that the safeness property of the queue element, given in the previous subsection is not true.

Informally, the problem can be described as follows: When an AckOut is received in response to the ReqOut signal, the AckOut signal travels via two different electrical paths — one involving three inverters and the other involving four gates. This creates a race condition and produces a glitch of about one gate delay on the ReqOut bus. Though this glitch may not always be able to drive the bus to create a spurious ReqOut, it has the potential to do so. However, this problem can be easily rectified by making the inverters slow or by putting five inverters on that path instead of three. The labelled state-transition graph for the corrected circuit is shown in figure 3.2.
The state-transition graph shown in figure 3.2. is only one portion of the complete state-transition graph for the FIFO Queue Element and corresponds to the initial state where both ReqIn and AckIn are both at logical-zero value and both ReqOut and AckOut are at logical-zero value. But the state in which both ReqIn and AckIn are at logical-zero and both ReqOut and AckOut are at logical-one can not be reached from this state-transition graph. In fact the state-graph with this situation as the initial condition is symmetric to the one shown and the complete state-transition graph consists of both of these components.
A sample run using the model checker is shown in figure 3.3. In the formula shown A stands for ∨, E for ⊃, I for ⊃, and ¬ for ∧ and → for →. Similarly, G, F, U and W will stand for G, F, U and W, respectively. The first component of "time:" is the cumulative time in 60th of a second; the second component is the portion of the cumulative time allocated to 'garbage collection'. The number to the right of each formula gives the time taken to determine the truth of the formula.

\[
\text{time: (1453 168)}
\]
\[
| = AG( (\neg \text{ReqIn} \& \text{AckIn}) \mid (\text{ReqIn} \& \neg \text{AckIn})) \&
(\neg \text{ReqOut} \& \neg \text{AckOut}) \mid (\text{ReqOut} \& \neg \text{AckOut})) \rightarrow
\]
\[
A[ (\neg \text{ReqIn} \& \text{AckIn}) \mid (\text{ReqIn} \& \neg \text{AckIn})] U
\]
\[
((\text{ReqOut} \& \text{AckOut}) \mid (\neg \text{ReqOut} \& \neg \text{AckOut}))]
\]
\[
< 7 \text{ secs.}
\]

\[
\text{time: (2263 300)}
\]
\[
| = AG( (\neg \text{ReqIn} \& \text{AckIn}) \mid (\text{ReqIn} \& \neg \text{AckIn})) \& (\neg \text{Full}) \rightarrow AF(A))
\]
\[
< 8 \text{ secs.}
\]

\[
\text{time: (2594 300)}
\]
\[
| = AG( (\text{Full}) \rightarrow AF( (\neg \text{ReqOut} \& \text{AckOut}) \mid (\text{ReqOut} \& \neg \text{AckOut})))
\]
\[
< 8 \text{ secs.}
\]

\[
\text{time: (3150 300)}
\]
\[
| = AG((\neg \text{ReqOut} \& \neg \text{AckOut}) \mid (\text{ReqOut} \& \neg \text{AckOut})) \rightarrow AF(\neg \text{Full}))
\]
\[
< 7 \text{ secs.}
\]

**Figure 3.3**

A sample run using the Model Checker.

4. Hierarchical Verification of Circuits.

The scheme given so far can be practical only for very small circuits. This is because it suffers from the problem that the state transition graph may have number of states, exponential in number of gates. However, this problem can be avoided, if circuits are verified in a hierarchical manner. That is, first small modules are verified and then bigger module is verified assuming that the smaller modules it is composed of are correct. Since at any hierarchical level, the number of small modules that a big module is composed of is relatively small, this method is amenable to proving correctness of large circuits without a large growth of the time complexity. Moreover, hierarchical verification permits the localization of faults to small submodules, thus allowing the designer to rectify the fault by redesigning the appropriate submodule.

In a hierarchical approach, the state transition graph for a circuit is built out of the descriptions of the constituent submodules. We obtain short a description of a module by using an operation called restriction. If \( L \) is the language for the module with a set of atomic propositions \( P \), corresponding to the input, output and internal nodes, then the operation restriction on \( L \), obtains a \( L' \) with atomic propositions \( P' \), corresponding to the input and the output nodes only.
Roughly speaking, the effect of restriction is to make the internal nodes invisible, since in building the state transition graph for the bigger module, we only require input-output behaviour of the constituent submodules. But when the internal nodes are made invisible, certain portions of the state graph will have same labelling of the atomic (input and output) propositions. The restriction operation defines exactly when such states can be collapsed into a single state.

Unfortunately, when we restrict a CTL structure to obtain a smaller structure, some formulæ that are true in the former structure may not be true in the restricted structure. However, by appropriately constraining CTL, we can show that the formulæ in the constrained logic have the desirable property that the truth properties of such formulæ are preserved with respect to the restriction operation. All of the formulæ used in section 3. have the desired syntax.

Let the CTL structure for $L$ be $\mathcal{M} = (S, R, \Pi)$. Let $P$ be the set of all atomic propositions in the language $L$, consisting of $I$, the set of atomic propositions corresponding to the inputs; $O$, the set of atomic propositions corresponding to the outputs and $\text{Int}$, the set of atomic propositions corresponding to the internal nodes of the circuit. That is $P = I \cup O \cup \text{Int}$. Let $L'$ be the language with the atomic propositions, $P' = I \cup O$. Define $\Pi P' : S \mapsto 2^{P'}$ to be the restriction of $\Pi$ to $P'$, i.e. $\forall s \in S [\Pi P'(s) = \Pi(s) \cap P']$. Now we can define a relation $\mathcal{E}$ ($\mathcal{E} \subseteq S \times S$) over the set of states of $\mathcal{M}$ such that

$s \mathcal{E} s'$ iff for some path $(s_0, s_1, \ldots, s_n)$ of $\mathcal{M}$, $n \geq 0$, $s = s_0$ and $s_n = s'$ and for each predecessor of $s_i$, $s'_i$ ($1 \leq i \leq n$), $\Pi P'(s'_i) = \Pi P(s_i)$

It is quite easy to see that $\mathcal{E}$ is a reflexive, asymmetric and transitive relation over $S$. The transitive closure of $\mathcal{E}$ can be defined as

$\mathcal{E}^* = \mathcal{E} \cup \mathcal{E}^2 \cup \mathcal{E}^3 \cup \ldots \cup \mathcal{E}^n \cup \ldots$

The $\mathcal{E}$-closure of a state $s$ is defined by $\mathcal{E}^*(s) = \{s' \mid s \mathcal{E} s'\} = \{s' \mid s \mathcal{E}^* s'\}$, since $\mathcal{E}$ is a transitive relation, i.e. $\mathcal{E}^* = \mathcal{E}$.

For a set of sets $\{u_j\}$, $\max(\{u_j\})$ will denote the set of all distinct sets in $\{u_j\}$ maximal under inclusion. We define a mapping $\varphi : S \mapsto 2^S$ such that for each $s \in S$,

$\varphi(s) = \max(\{H_i \mid s \in H_i \land \exists s_t \in \mathcal{E}^*(s_t) = H_i\})$,

i.e. $\varphi(s)$ is the set of maximal $\mathcal{E}$-closures containing $s$. We consider the following subsets of $S$,

$\Delta = \varphi(S) = \bigcup_{s \in S} \varphi(s)$.

Since every element $s \in S$ belongs to at least one subset $H_i$ of $\Delta$, $\Delta$ is called a decomposition of $S$ and the $H_i$'s are called the blocks of the decomposition. In a block $H_i$, the relation $\mathcal{E}$ defines a partial order over the set of states of $H_i$. We will say $s$ dominates $s'$, if $s \mathcal{E} s'$. We define the dominant states of $H_i$, $\text{dom}(H_i)$ as the set of states that dominate every other states in $H_i$.

The decomposition $\Delta$ naturally leads to a substructure of a model $\mathcal{M}$ (notation $\mathcal{M}' = (S', R', \Pi') = \mathcal{M}/\Delta$). The states of $\mathcal{M}'$ will be the blocks of $\Delta$. A block $H_i$ of $\Delta$, when considered as an element of $S'$, will be denoted by $\overline{H_i}$. Let $R' (R' \subseteq S' \times S')$ be the total binary relation on $S'$, corresponding to $R$ and induced by the decomposition $\Delta$ i.e.

$(\overline{H_i}, \overline{H_j}) \in R'$ iff for some $s_i \in H_i$, $s_j \in H_j$, $(s_i, s_j) \in R$.

Similarly, let $\Pi' : S' \mapsto 2^{P'}$ be the mapping corresponding to $\Pi$ and induced by the decomposition $\Delta$, i.e.

$\Pi'(\overline{H_i}) = P' \cap \bigcap_{s \in H_i} \Pi(s)$.
The model $\mathcal{M}' = (S', R', I_1')$ is called a restriction of $\mathcal{M} = (S, R, I_1)$ with respect to $P' \subseteq P$. From the definition it is easy to prove that

**Lemma 4.1.** If $\mathcal{M}' = (S', R', I_1')$ is a restriction of $\mathcal{M} = (S, R, I_1)$, with respect to $P'$, then

(i) For all $\langle \overline{I}_i, \overline{I}_j \rangle \in S'$, $\langle \overline{I}_i, \overline{I}_j \rangle \in R'$ iff there is a path from $s_i'$ to $s_j'$ ($s_i' \in \text{dom}(\overline{I}_i), s_j' \in \overline{I}_j$) such that $(s_0 = s_0, \ldots, s_k, s_{k+1}, \ldots, s_m = s_j')$ in $\mathcal{M}$ and for some $0 < k < m$, $s_0, \ldots, s_k \in H_i$ and $s_{k+1}, \ldots, s_m \in H_j$.

(ii) For all $s$ such that $s \in H$, $\Pi'(\overline{I}) = \Pi(s) \cap P'$.

**Proof.** Trivial. Directly follows from the definitions.

We extend the operation of restriction to a path in a CTL structure. Let $p = (s_0, \ldots, s_n, s_{n+1}, \ldots)$ be a path in $\mathcal{M}$. Then define

$$
\mathcal{R}_{P'}(p) = \begin{cases} 
(\overline{I}_0, \overline{I}_0, \ldots, \overline{I}_0), & \text{if } (s_0, \ldots, s_n) \text{ is a finite prefix of } p \text{ such that } s_0, \ldots, s_n \in H_0 \text{ and } s_{n+1} \notin H_0; \\
\text{Otherwise}, & \text{and } s_0, \ldots \in H_0.
\end{cases}
$$

**Lemma 4.2.** Let $(s_0, \ldots, s_n, s_{n+1}, \ldots)$ be a path in $\mathcal{M}$. Then $\mathcal{R}_{P'}(s_0, \ldots, s_n, s_{n+1}, \ldots)$ is a path in $\mathcal{M}'$. Conversely, if $(\overline{I}_0, \overline{I}_1, \ldots)$ is a path in $\mathcal{M}'$ and $s_0 \in \text{dom}(H_0)$, then there is a path $(s_0, s_1, \ldots)$ in $\mathcal{M}$ and $\mathcal{R}_{P'}(s_0, s_1, \ldots) = (\overline{I}_0, \overline{I}_1, \ldots)$.

**Proof.** From definition and lemma 4.1.(i).

In the following theorem, we show that there are CTL formulae whose truth-properties are not preserved with respect to restriction.

**Theorem 4.1.** There exists a CTL structure $\mathcal{M} = (S, R, I_1)$ and a formula $\mathcal{F}$ where $\mathcal{F}$ is a CTL formula such that $\mathcal{M}, s_0 \models \mathcal{F}$ but $\mathcal{M}', \overline{I}_0 \not\models \mathcal{F}$, and $s_0 \in \text{dom}(H_0)$.

**Proof.** The counter-examples involving formulae of the form $\forall XP, \exists XP$ and $\forall[\exists FP_1 U P_2]$, are given in [MC83].

However, there exists a large subclass of CTL formulae with the desirable property that if a formula in this subclass is satisfiable in the unrestricted CTL structure, $\mathcal{M}$, then it is satisfiable in the CTL structure, $\mathcal{M}'$ obtained by restriction. We call this subclass CTL'. Given a set of atomic propositions $P$:

1. Every atomic proposition $P \in P$ is a propositional formula in CTL'.
2. If $f_1$ and $f_2$ are propositional formulae in CTL', then so are $\neg f_1, f_1 \land f_2$.
3. If $f_1$ is a propositional formula and $f_2$ is a CTL'-formula, then $\forall[f_1 U f_2]$ and $\exists[f_1 U f_2]$ are CTL'-formulae.

**Theorem 4.2.** Let $\mathcal{F}$ be a CTL'-formula in $L'$. Then $\mathcal{M}, s_i \models \mathcal{F}$ iff $\mathcal{M}', \overline{I}_i \models \mathcal{F}$, where $s_i \in \text{dom}(H_i)$.

**Proof.** By induction on the structure the CTL formula $\mathcal{F}$ and the Computation Tree rooted at $s_i$. See [MC83] for a full proof.
COROLLARY 4.1. Let $F$ be a CTL formula in $L'$. Then

$$M, s_0 \models F \iff M', \overline{H_0} \models F,$$

where $s_0 \in \text{dom}(H_0)$.

Proof. Corollary to theorem 4.2. 

With each model $M$, one can associate an automaton such that its states and transitions are same as that of $M$, but the transitions are additionally labelled with the set of input signals that cause the transition and the set of output signals associated with the transition. Let $A$ and $A'$ be the automata associated with the models $M$ and $M'$, respectively. It can be easily shown that the relation $\varphi$ is a weak homomorphism of $A$ onto $A'$ and hence $A'$ is a covering of $A$ [G168]. The above result can be strengthened, if we notice that

$$\varphi^{-1}M^A_{e\sigma^*} = M^A'_{e\sigma^*}, \quad \text{and} \quad \varphi^{-1}N^A_{e\sigma^*} = N^A'_{e\sigma^*},$$

where $M^A$ and $M^A'$ are the transition functions and where $N^A$ and $N^A'$ are the output functions of the automata $A$ and $A'$, respectively.

THEOREM 4.3. Let $A$ and $A'$ be the automata associated with the models $M$ and $M'$, respectively. Then the models $M$ and $M'$ are input-output equivalent in the sense that for a sequence of input signals, $x$,

$$N^A_x \subseteq \varphi N^A'_x,$$

and

$$\varphi^{-1}N^A_x = N^A'_x,$$

where $N^A$ and $N^A'$ are the output functions of the automata $A$ and $A'$, respectively.

Proof. Let $x = a_1a_2...a_k$. Then

$$\varphi^{-1}M^A_x = \varphi^{-1}M^A_{e\sigma^*}M^A_{a_2}...M^A_{a_k}$$

$$= M^A_{e\sigma^*} \varphi^{-1}M^A_{a_2}...M^A_{a_k}$$

$$= M^A'_{e\sigma^*}M^A'_{a_2}...M^A'_{a_k} = M^A'_{e\sigma^*} = M^A' \varphi^{-1}$$

Similarly,

$$\varphi^{-1}N^A_x = \varphi^{-1}M^A_{e\sigma^*}M^A_{a_2}...M^A_{a_k}N^A_{a_k}$$

$$= M^A'_{e\sigma^*}M^A'_{a_2}...M^A'_{a_k-1} \varphi^{-1}N^A_{e\sigma^*}$$

$$= M^A'_{e\sigma^*}M^A'_{a_2}...M^A'_{a_k-1}N^A'_{e\sigma^*} = N^A'_x$$

But since $\varphi^{-1} \supseteq I_{G_A}$ we have

$$\varphi^{-1}N^A_x = N^A'_x \Rightarrow \varphi N^A'_x = \varphi N^A_x$$

$$= I_{G_A}N^A_x \subseteq \varphi N^A'_x$$

$$= N^A_x \subseteq \varphi N^A'.$$

Hence we see that even if the operation of restriction does not preserve all the CTL formulae, the restricted model is equivalent to the original model in terms of its behaviour.

†We represent the composition of functions $\varphi_1 : D_1 \rightarrow D_2$ and $\varphi_2 : D_2 \rightarrow D_3$ by $\varphi_1 \varphi_2 : D_1 \rightarrow D_3$. The transition function is $M : \Sigma \rightarrow (S \rightarrow S)$ and the output function is $N : \Sigma \rightarrow (S \rightarrow \Theta)$. 
We show how to build $M'$ from $M$ in the following three steps. $M'$ is essentially a restriction of $M$ with additional optimizations and labelling of the transitions of the state-transition graph.

**step 1.** Relabel the vertices and the edges of the CTL structure $M$. (a) Label each state by the subset of the propositions involving only the inputs and the outputs of the module. (b) Label the edges between two states with the same set of atomic propositions, by $\epsilon$.

**step 2.** Construct the blocks of $M$, by first determining the dominant states using a depth first search over the underlying graph. Build $M'$ by replacing each block by a single state. The graph can be optimized further by collapsing the "indistinguishable nodes" (i.e. nodes with the same label and successor states) into single node.

**step 3.** Label the edges of the graph by the set of input signals that causes the transition and the set of output signals associated with the transition.

This construction is illustrated by taking the restriction of the state-transition graph for the FIFO Queue Element shown in figure. 3.2. The states shown in groups are the blocks constructed in step 2. The resulting labelled state-transition graph is shown in figure. 4.1.

---

*figure. 4.1.*

*The Restricted State Transition Graph.*
It should be mentioned that since we combine successive states in the operation of step 2, the restricted model may not be a unit-delay model even if the original unrestricted model was so. This notion is essentially captured in Theorems 4.1. and 4.2. However, this does not pose a problem, since good design methodology forces the designer not to make the modules at higher level in the hierarchy speed-dependent. Moreover, since a speed-dependent circuits must be small enough to fit in an equipotential region and equipotential regions must be small enough that the potential on any wire in this area will equalize in a "short" time for any large circuit, the modules at higher level have to be speed-independent [MC80].

As the first step for verifying the correctness of a circuit using a hierarchical approach, we construct a CTL structure for a module at some hierarchical level, using the CTL structures for the submodules at the immediately lower level. In order to avoid building large-sized CTL structures, we use the restriction operation on the CTL structures of the submodules and obtain smaller descriptions of these. Moreover, the transitions of the state-transition graph are additionally labelled with the associated set of input signals and set of output signals, as explained earlier in this section.

Given two submodules A and B which are used to build a module C at a higher level by connecting the inputs and outputs of A and B, we show how to build a CTL structure for the module C using an operation called "composition". It can be shown that the composition operation is commutative and associative and hence can be generalized easily to the case where a module consists of more than two submodules. The reader may note a close analogy between the operations we define and the operations defined in [MI80].

Let the restricted models of A and B be $M'_A = (S'_A, R'_A, I'_A)$ and $M'_B = (S'_B, R'_B, I'_B)$, respectively.

The CTL structure of $C = A \circ B$ is given by $M_C = M_{A \circ B} = (S_{A \circ B}, R_{A \circ B}, I_{A \circ B})$, where $S_{A \circ B} = S_A \times S_B$. The assignment function $I_{A \circ B} : S_{A \circ B} \rightarrow 2^{P_A \cup P_B}$ is defined by $I''(s_A) = I'(s_A) \cup I''(s_B)$ where the state $s_{A \circ B} = (s_A, s_B)$. The initial state of $M_C$ is $s_0(A \circ B) = (s_{0A}, s_{0B})$.

The transition relation $R_{A \circ B}$ ($R_{A \circ B} \subseteq S_{A \circ B} \times S_{A \circ B}$) is defined as follows. Assume that there is a transition $(s_{1A}, s_{2A}) \in R_A$ such that $(s_{1A}, s_{2A})$ is labelled with the input set $\alpha$ and output set $\beta$. Similarly assume that there is a transition $(s_{1B}, s_{2B}) \in R_B$ such that $(s_{1B}, s_{2B})$ is labelled with the input set $\gamma$ and the output set $\delta$. Then in the CTL structure for $C$, there will be transitions, $((s_{1A}, s_{1B}), (s_{2A}, s_{2B})) \in R_{A \circ B}$, corresponding to input, $\alpha$ and output, $\beta$; and $((s_{1A}, s_{1B}), (s_{1A}, s_{2B})) \in R_{A \circ B}$, corresponding to input, $\delta$ and output, $\gamma$. Moreover, if $\gamma \subseteq \beta$ or $\alpha \subseteq \delta$, then there will be an additional transition from $((s_{1A}, s_{1B}), (s_{2A}, s_{2B})) \in R_{A \circ B}$, corresponding to input, $\alpha \cup \gamma$ and output, $\beta \cup \delta$.

The step of constructing the successor states for $(s_{1A}, s_{1B})$ can be thought of as simulating $C$ at $(s_{1A}, s_{1B})$ for all possible sets of inputs and can be easily incorporated into algorithm 2.1. Now various properties of $C$ with respect to the model $M_C$ can be determined using the model checker algorithm, as explained in the earlier sections.

5. Conclusion.

We have shown that it is possible to do automatic verification of asynchronous circuit efficiently. We have also indicated how this method can be extended to do hierarchical verification of large and complex circuits. We believe that this approach may eventually turn out to be quite practical.
However, there are many problems that need to be addressed before this approach is made feasible in practice. In this paper we have used a unit-delay model for the circuit. Similarly, it is quite easy to use a steady-state model, in which each state in the state-transition graph corresponds to a stable state and only in response to an input change does a state change occur. While the steady-state model is useful for speed-independent self-timed circuits, the unit-delay model is needed to model properties of a speed-dependent circuit. Unfortunately, even for the speed-dependent circuits the assumption that each gate has one unit gate-delay is rather unrealistic, because two similar gates may have different delays depending on process variations, fan-outs of a gate etc. Moreover, because of various capacitive effects, the delay associated with a 0-to-1 transition is not equal to the one associated with a 1-to-0 transition. It is felt that it is necessary to find models that capture these properties better. Also, we do not know how to handle the effect of large fan-out, charge sharing etc. In addition, we felt that CTL is rather weak for succinctly expressing many properties of circuits. A notation based on temporal intervals [HIM83] may be more suitable for this purpose.

An interesting area for future research is the usefulness of restriction operation in the context of hierarchical verification. We have defined a "restriction" operation and shown that the truth-properties of the CTL-formulas are preserved with respect to the operation of restriction. It appears that any weaker version of "restriction" will not result in any substantial reduction of the size of the CTL structures and hence will make hierarchical verification rather expensive. On the other hand, it seems any stronger version of "restriction", will severely limit the class of CTL formulas that will be preserved with respect to restriction.

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7. References.


