Programming Reconfigurable Computers
February 23, 1998

- Wednesday
- Projects
- What we will cover
- Data Parallel
- Silage

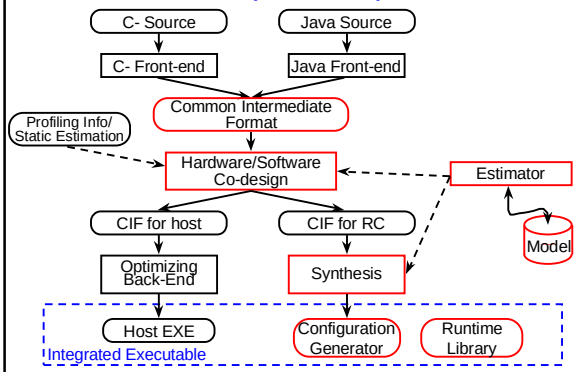
Programming Approaches

- general purpose HDL
- RC Specific languages:
  CVHASM, LDG, PERLDC, …
- Restricted general purpose languages
  DIC
- General Purpose programming languages
- Another Axis: Parallel or Serial

Compiling for RC

- Partitioning
- Mapping
  - Software pipelining
  - Systolic Techniques
  - Microcode techniques
  - super-blocks
  - trace-scheduling
- Back-end techniques
- Synchronization/Communication

A Sample Compiler



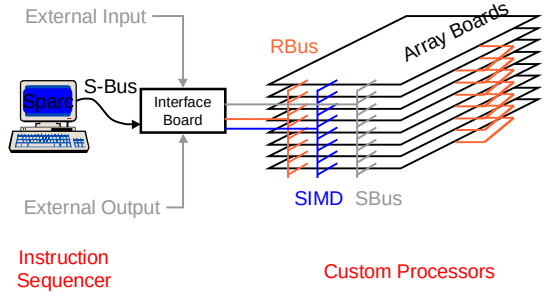
The Programming Model

- Programming language introduces a model of the machine.
- The model should(?) abstract away
  - host/fabric interface
  - FPGA details
  - Timing details - the clock
- The model should allow for efficient programs

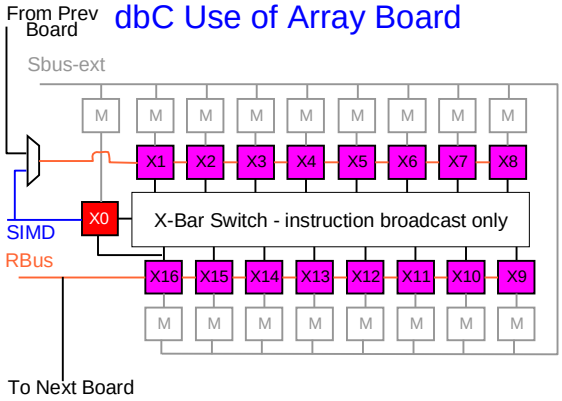
Data Parallel Model and Splash

- SIMD execution model
- N procs arranged in 1-d array.
- Variable bit-width fixed-point data types.
- Communication: nearest neighbor
- Program by decomposition.
- Reduction operations

dbC use of Splash-2



dbC Use of Array Board



Programming Splash-2

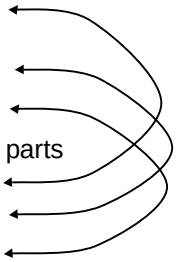
- dbC program generates:
  - Host - sequencer
  - Interface Board (XL & XR) - fixed
  - Array Board
    - X0 - fixed + reduction operators
    - X1-X16 - the program
    - TI Chips - fixed

Compilation

- dbC ⇒ C
- Determine dependencies and create multi-cycle instructions.
- synthesize datapath for each SIMD instruction.
- Combine datapaths into a single unit - a PE. Includes decoders etc. Multiple PEs on a chip
- Create synchronization code - i.e., **`SPLASH_INSTRUCTIONS`**
- Synthesize communication code
  - Nearest neighbor code
  - global operations

Template Based Approach

- Each of X1-X16 is broken up into 4 parts:
  - instruction decoder
  - PEs
  - Reduction control
  - Reduction operators
- X0 is broken into three parts
  - instruction decode
  - reduction control
  - reduction operators



Communication

- To Array: 2 cycles
  Uses instructions w/intermediate data
- From 1 PE in Array: Uses global or
- From Array: Uses R-Bus
- PE-PE: 4 cycles!
  3 reads + 1 write

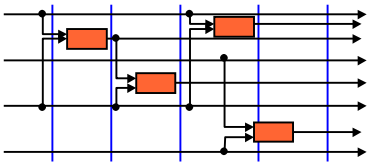
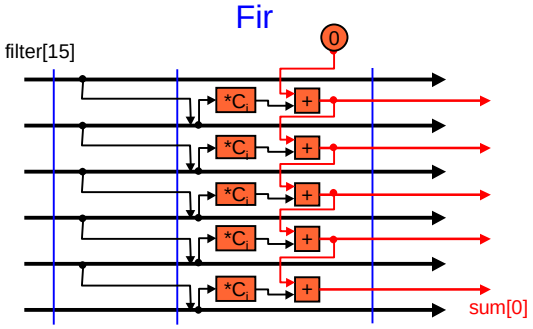
Reduction Operators

- Bitwise reduction operators
- MIN, MAX, OR, XOR, AND, ?
- 2 stage operation:
  - compute operation on each chip
  - combine among chips
- Pipelined. Is this important?

dbC Summary

Silage Machine Model

- fixed point values
- infinite streams of data
- infinite number of processors
- k cycle per operation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