Alpha 21264 Supplement
CS 740
Oct. 14, 1998

Extracted from

“Digital 21264 Sets New Standard”

Microprocessor Report, Oct. 28, 1996

Branch/Jump Target Prediction

Integrated into instruction cache

- **64KB, consisting of 4K lines, each 16B (4 instructions)**
- **Each cache line carries 12b "next line" + 1b "next set" predictor**
  - 6.5KB total
  - Set to predicted target if line contains predicted-taken branch
  - Set to next sequential line otherwise

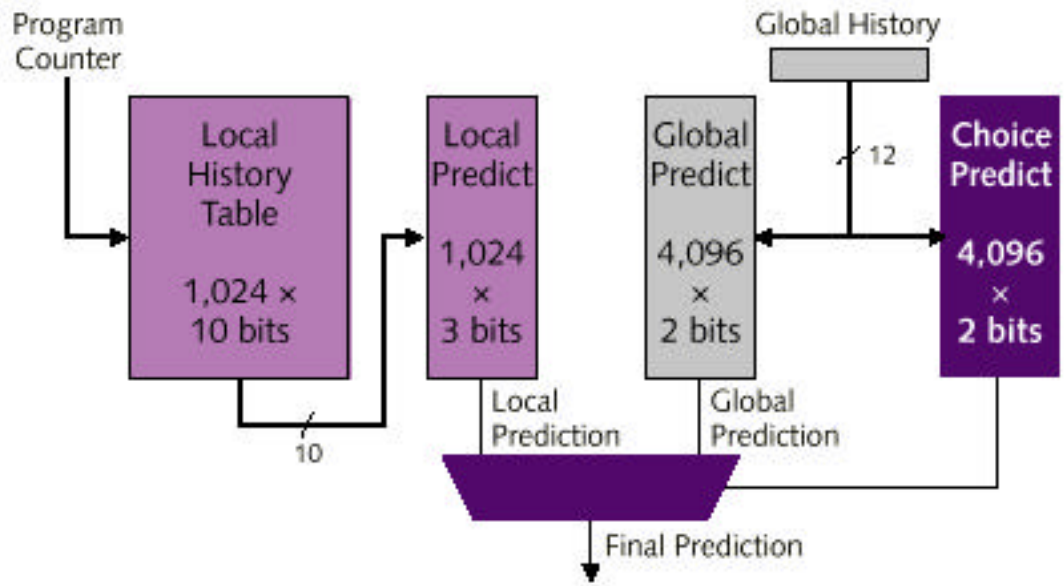
Predicting Procedure Return Target

- **Maintain stack of return points for 32 most recent calls**
- **100% accuracy as long as no non-standard returns**

Alignment issues

- **Taken branch best if instruction address of form** $4i + 3$
  - Will use other 3 instructions in line
- **Branch target should have address of form** $4i$
  - First instruction in line

Branch Prediction Logic



- **Purpose: Predict whether or not branch taken**
- **35Kb of prediction information**
- **2% of total die size**
- **Claim 0.7--1.0% of all instructions are mispredicted branches**
  - But only 1/6 instructions are branches in the first place

  ➜4.2–6.0% mispredication rate

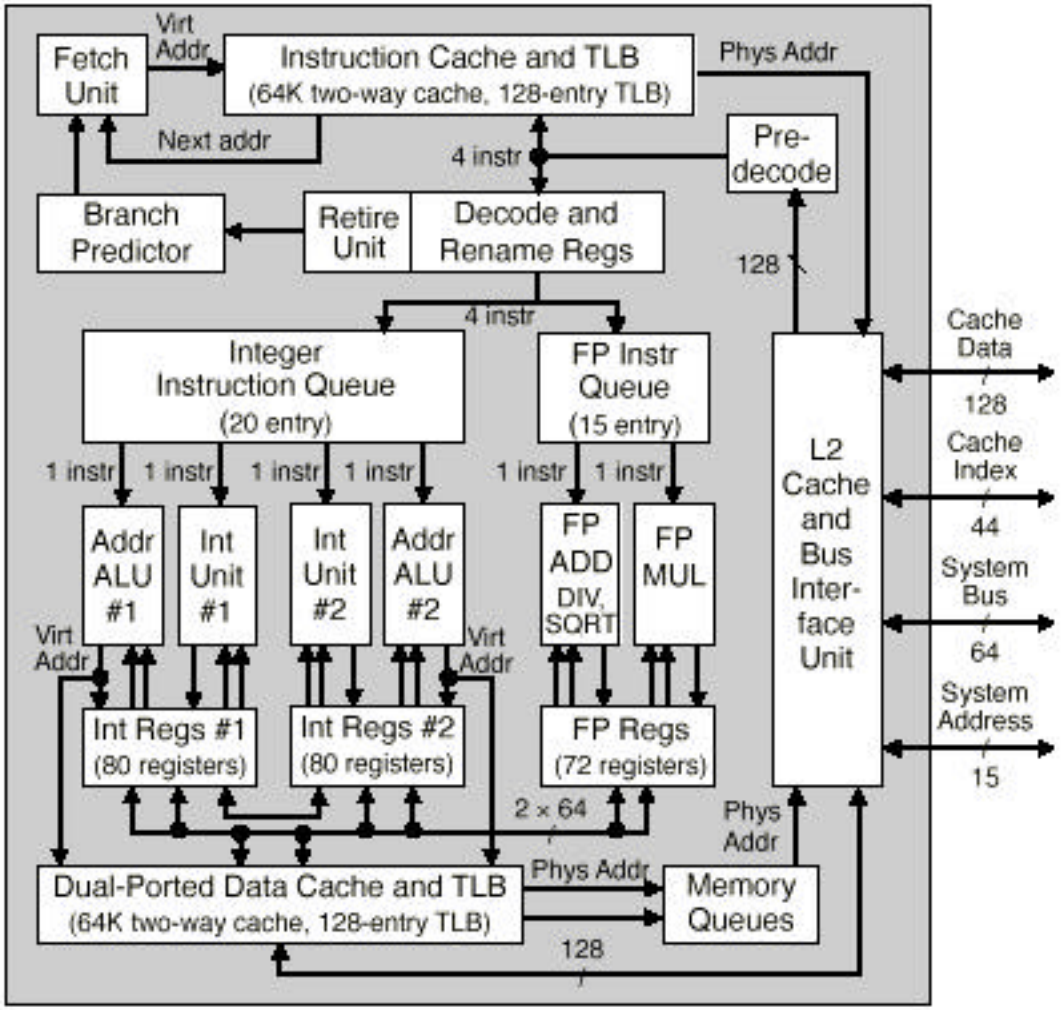
Block Diagram

4 Integer ALUs

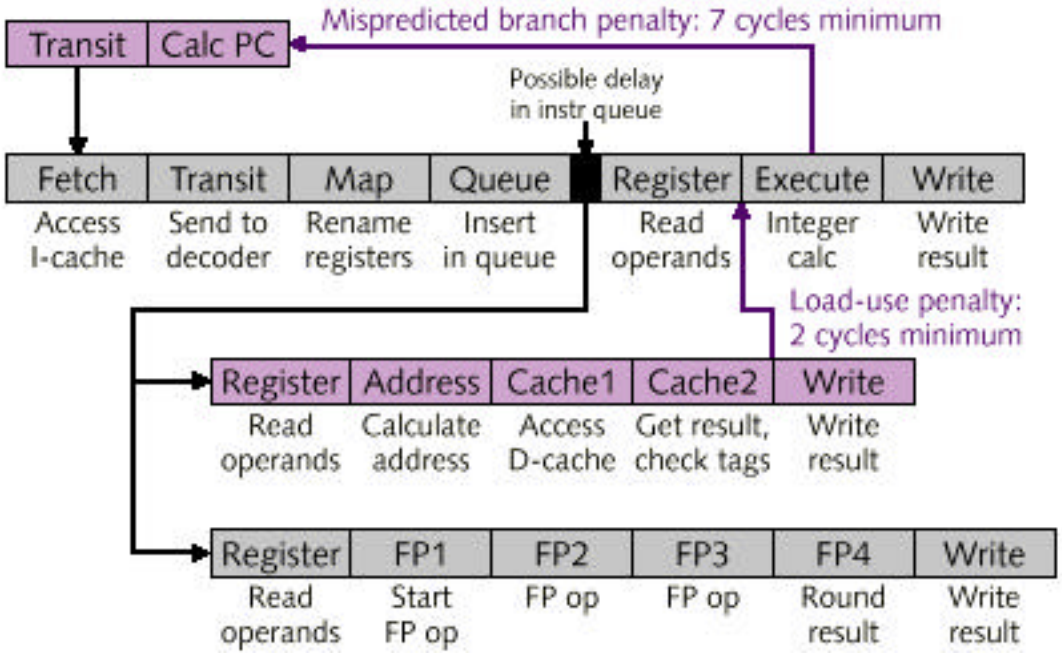
- **Each can perform simple instructions**
- **2 handle address calculations**

Register Files

- **32 arch / 80 physical Int**
- **32 arch / 72 physical FP**
- **Int registers duplicated**
  - Extra cycle delay from write in one to read in other
  - Each has 6 read ports, 4 write ports
  - Attempt to issue consumer to producer side



Pipeline Behavior



- **Misprediction adds 0.1 to SpecInt95 CPI**
  - Yielding 0.5

Interesting Facts

Very Complex Chip

- **15.2 M transistors total**
- **6 M for CPU core**
  - Vs. 4.2M for Intel PentiumPro

Interesting Memory Subsystem

- **Have found in past that memory bandwidth is major bottleneck**
  - CPU often “starved” waiting for loads & stores
  - Not reflected in SPEC benchmarks
    - » Tend to fit entirely in cache

Measured Performance

Machines

- **Alpha 21264 @ 575 MHz**
  - (64+64) KB L1, 4MB L2, 512 MB main memory
- **Intel Pentium II @450 MHz**
  - (16+16) KB L1, 512KB L2, 64 MB main memory

SPEC Results

- **Alpha**
  - June ‘98
  - SpecInt95: 30.3
  - SpecFP95: 47.7
- **Intel**
  - August ‘98
  - SpecInt95: 17.2
  - SpecFP95: 12.7