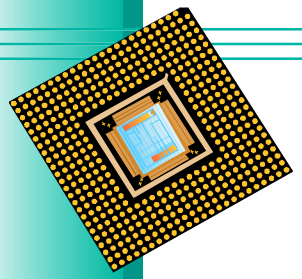


The 21264: A Superscalar Alpha Processor with Out-of-Order Execution

Jim Keller

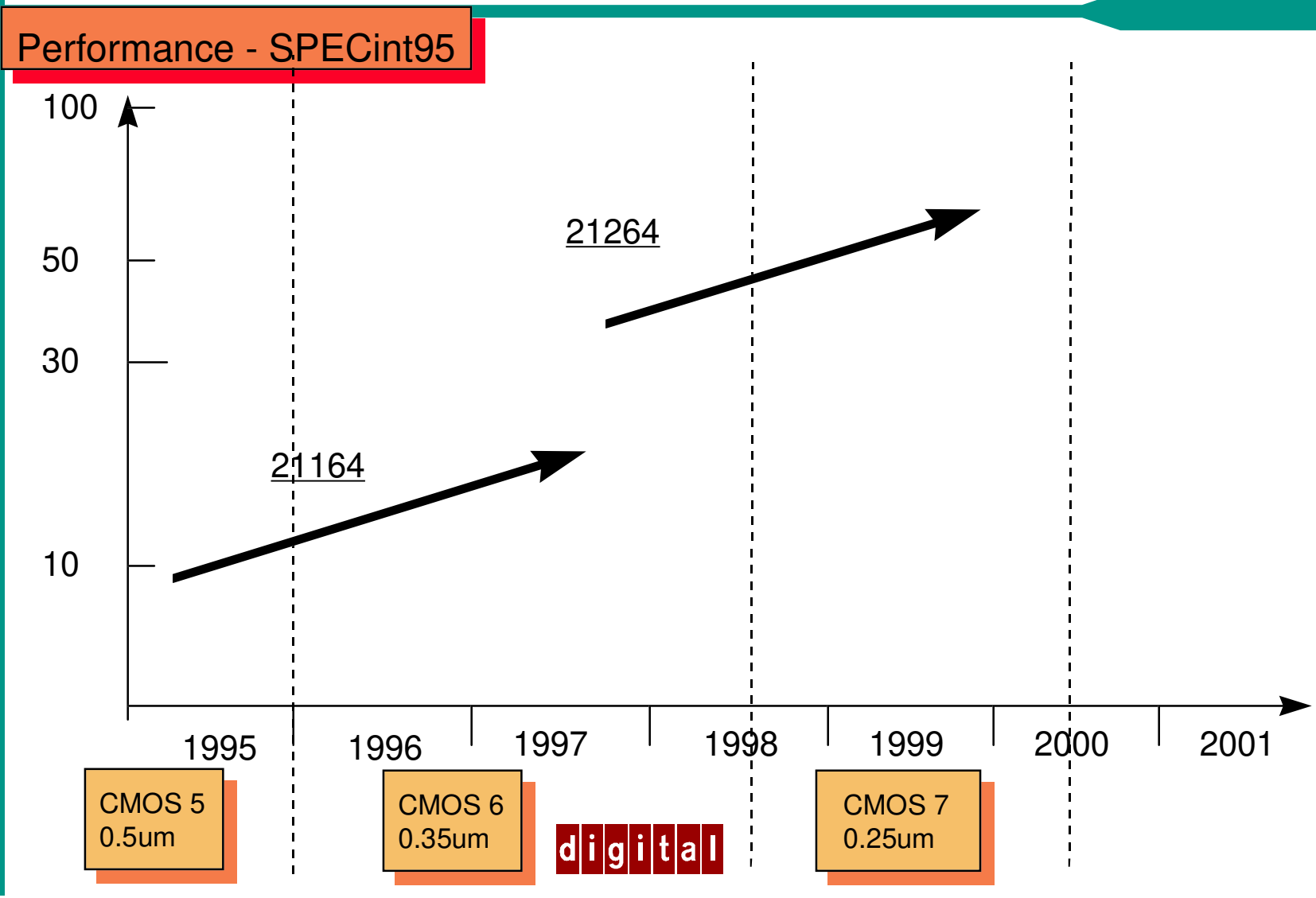
Digital Semiconductor

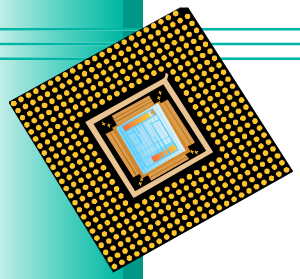
Digital Equipment Corp.

Hudson MA

digital

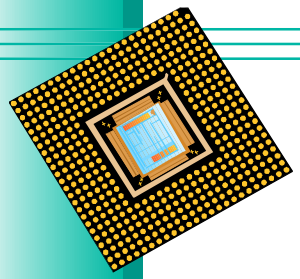
Alpha Microprocessor Roadmap





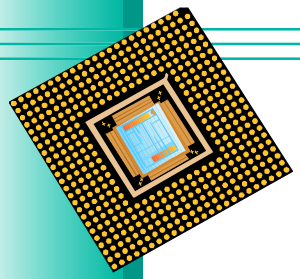
Highlights

- Continued Performance Leadership
  - Est. SPECint95 of **30+** and SPECfp95 of **50+**
  - Spectacular memory bandwidth
- Architectural, circuit and process leadership achieve 500 MHz operation in 0.35u CMOS
- Four-way Out-of-Order Execution
- Implements Alpha Motion Video Instructions
  - MPEG2 encode in realtime

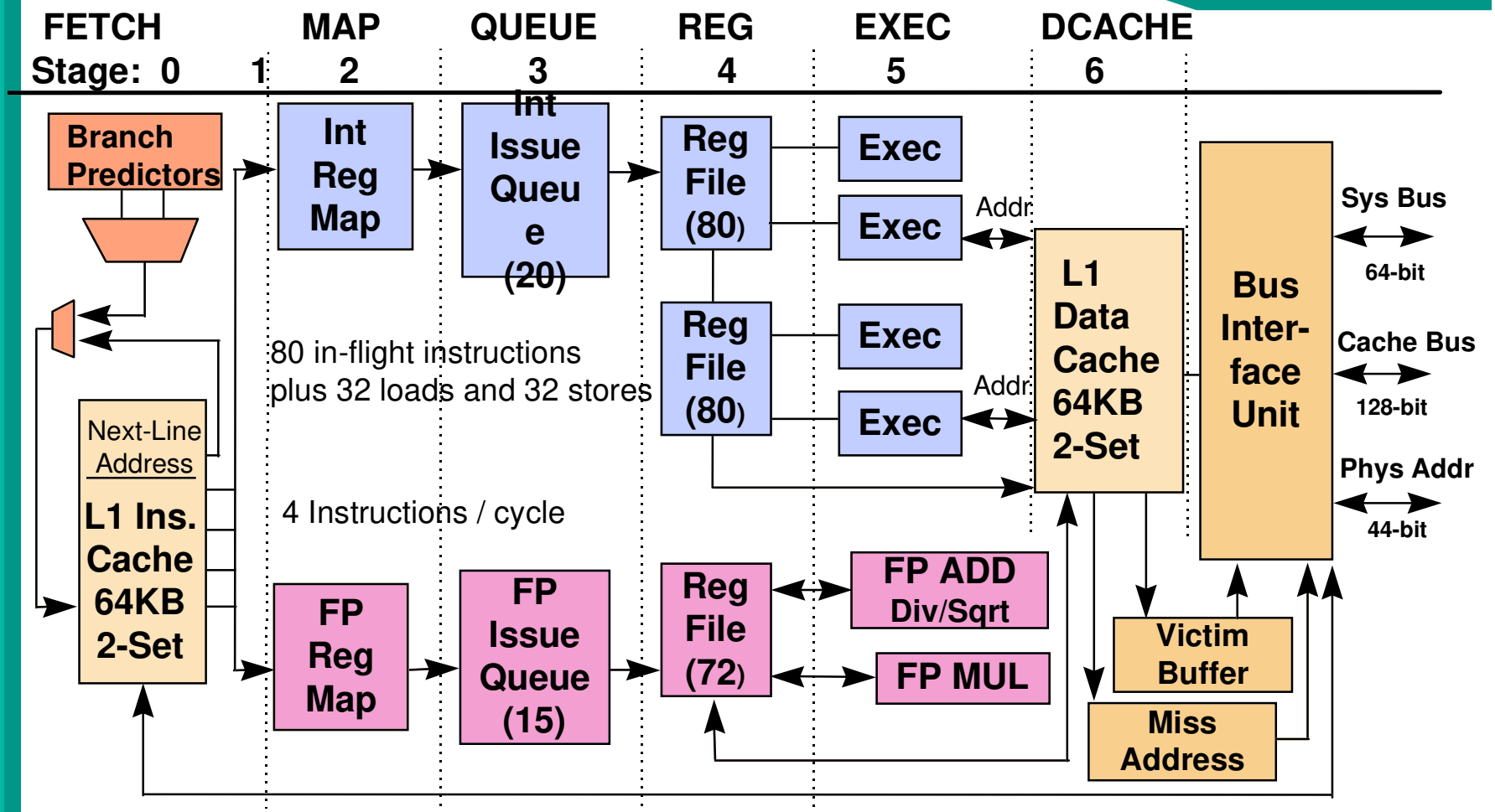


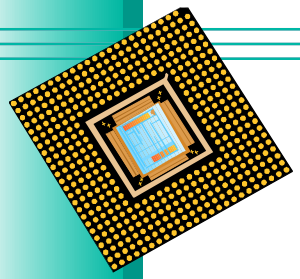
Alpha 21264 Characteristics

Feature	Description
Process Technology	CMOS 6 - 6 layer metal
Min. Feature Size	0.35µ drawn
Transistor Count	15.2 Million
Frequency	500+ MHz
Power	60 Watts
Die Size	3.0 cm^2
Issue Rate	4 Integer 2 Floating Point
L1 Instruction Cache	64KByte 2-way Set Associative
L1 Data Cache	64KByte 2-way Set Associative
Package	588 PGA
Samples	Q1 97
Volume	H2 97

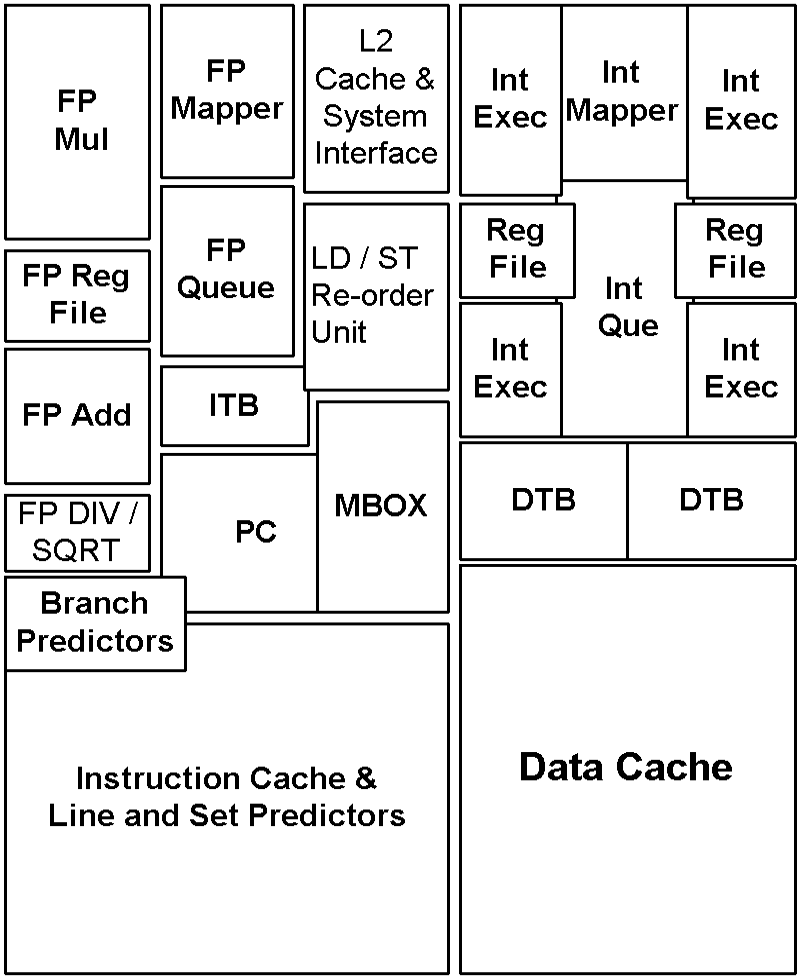


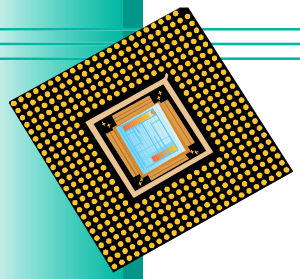
Alpha 21264: Block Diagram





Alpha 21264 Floor Plan





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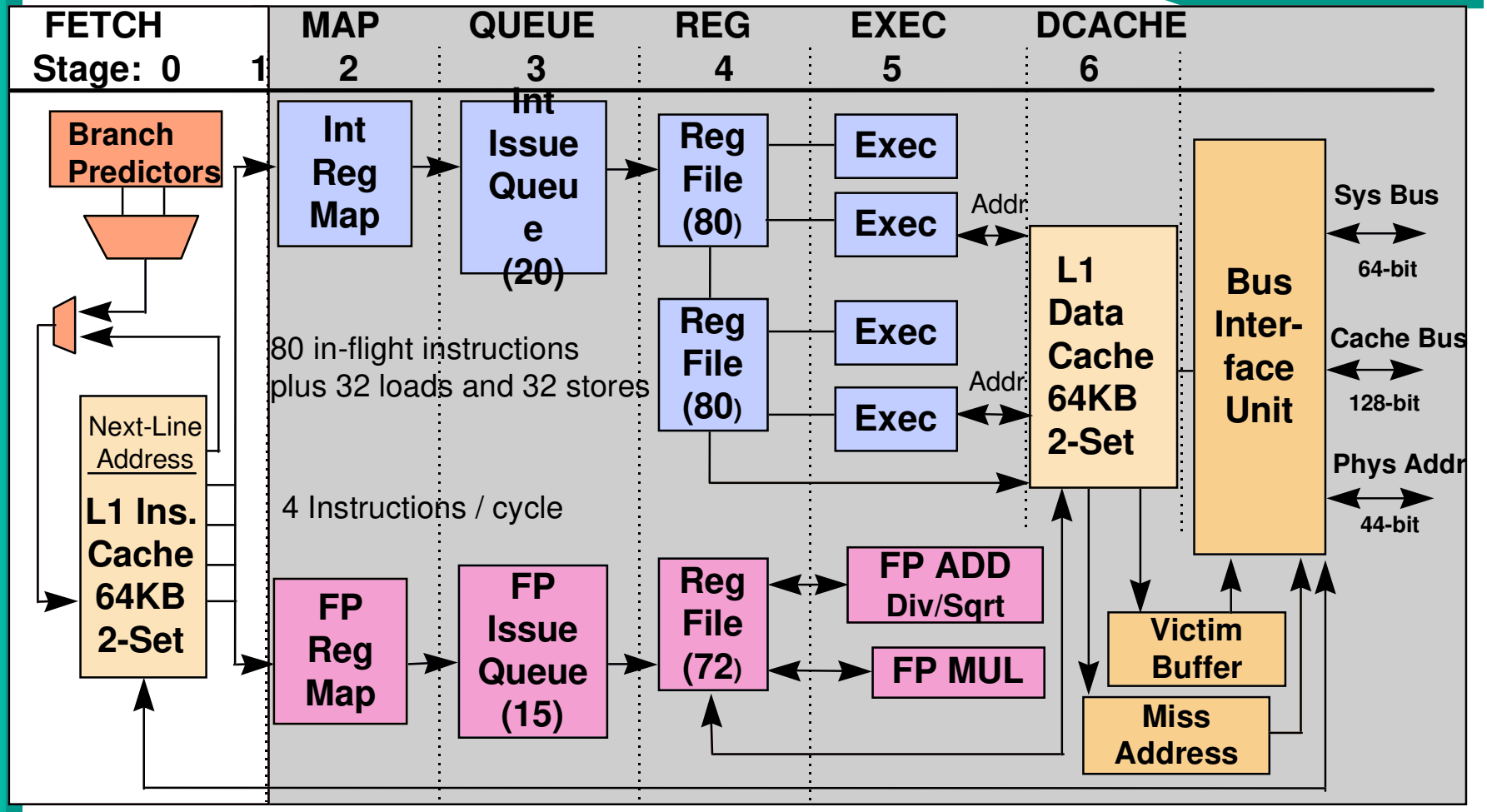
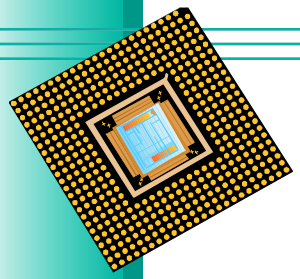
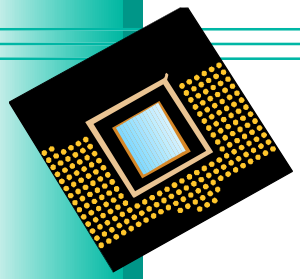


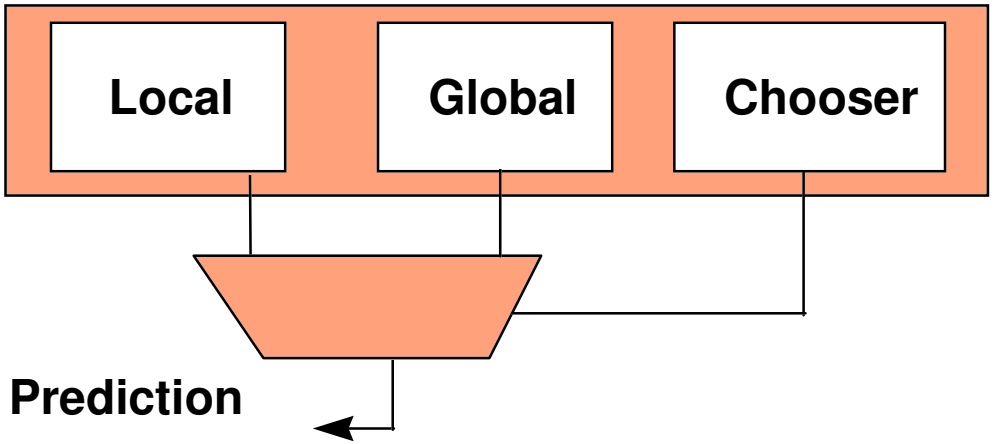


Fetch Stage: Fetch and Set Predictors

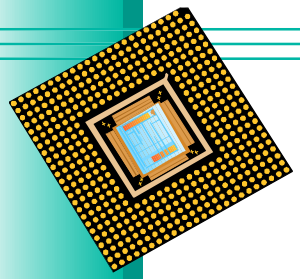
- Four instructions plus a ***Next-fetch predictor*** are fetched per cycle from the instruction cache
  - Pipelined branch predictor runs in parallel
- ***Next-fetch predictor*** addresses the cache next cycle
  - Eliminates branch bubbles
  - Learns dynamic jump targets for DLL's
- Set Predictor stores next-icache set (one of two) in current icache line
  - Enables associative cache at high speed



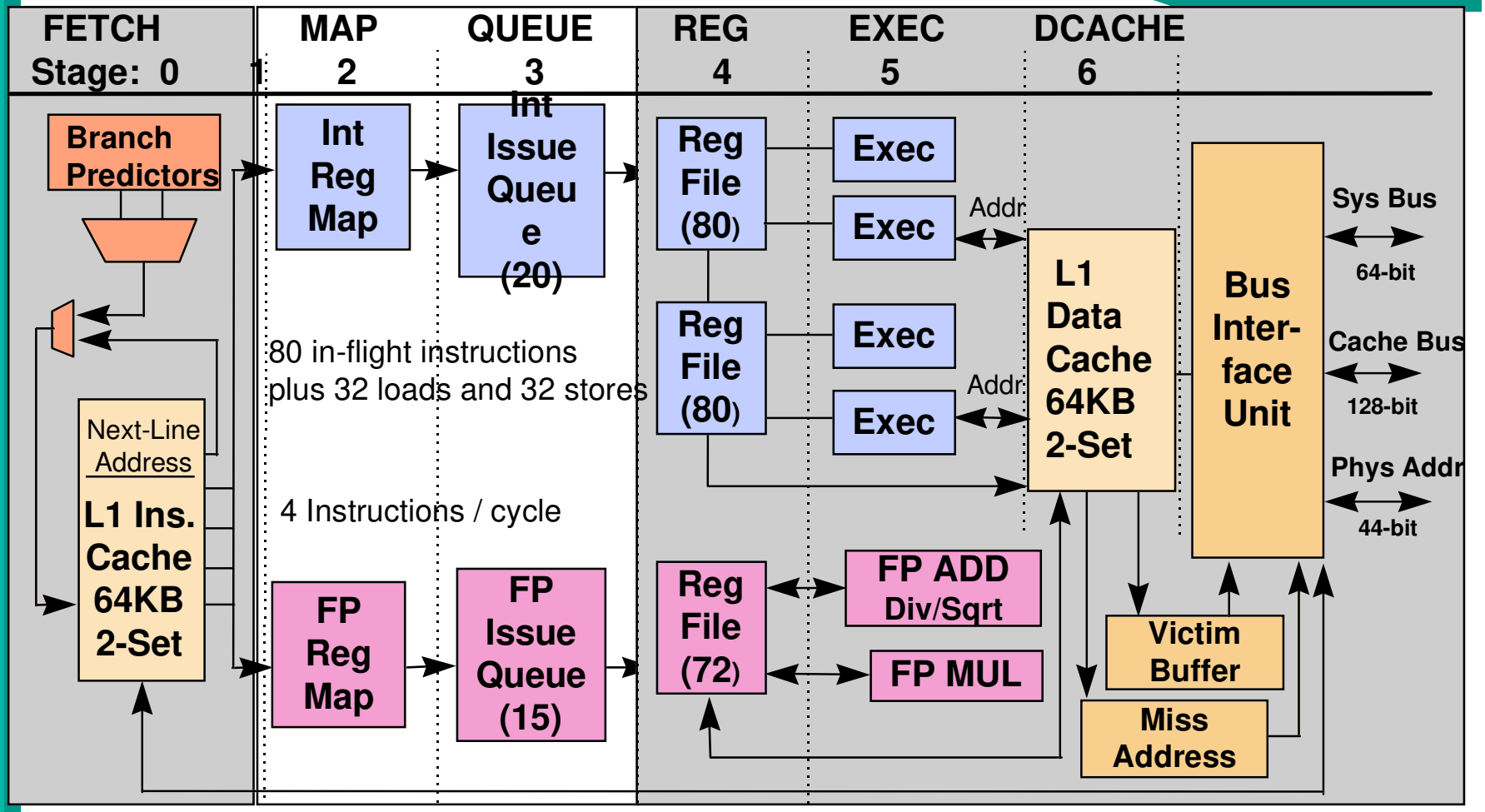
Fetch Stage: Branch Prediction

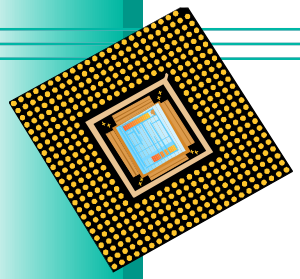


- Some branch directions can be predicted based on their past behavior: *Local Correlation*
- Others can be predicted based on how the program arrived at the branch: *Global Correlation*
- 21264 implements both methods and dynamically applies the best one



Alpha 21264: Block Diagram

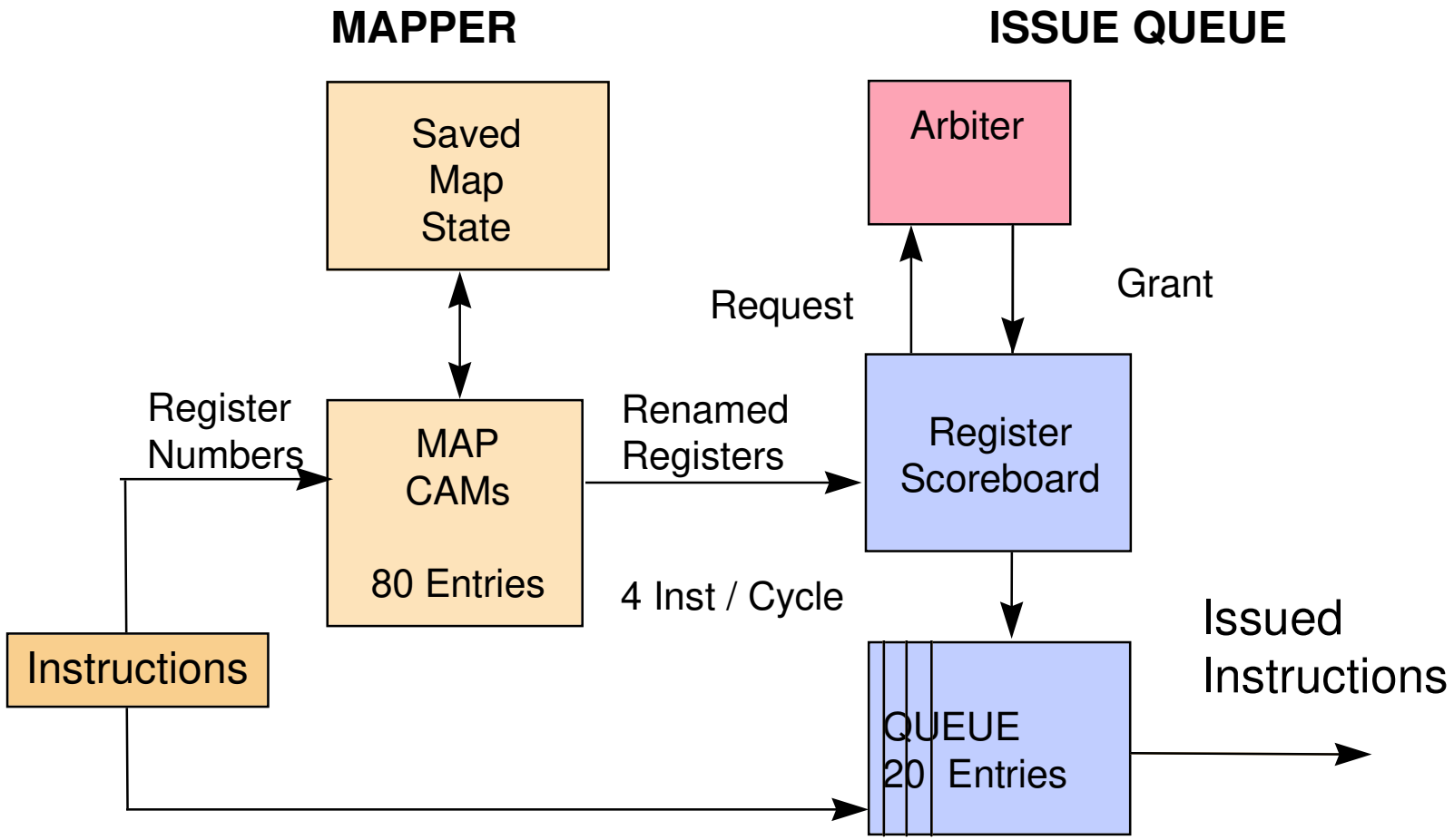


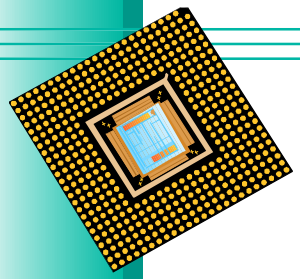


Mapper and Queue Stages

- Mapper:
  - Rename 4 instructions per cycle (8 source / 4 dest)
  - 80 int + 72 fp physical registers
- Queue Stage:
  - Instructions issued out-of-order when data ready
  - Instructions leave the queues after they issue
  - Integer: 20 entries / Quad-Issue
  - Floating Point: 15 entries / Dual-Issue

Map and Queue Stages





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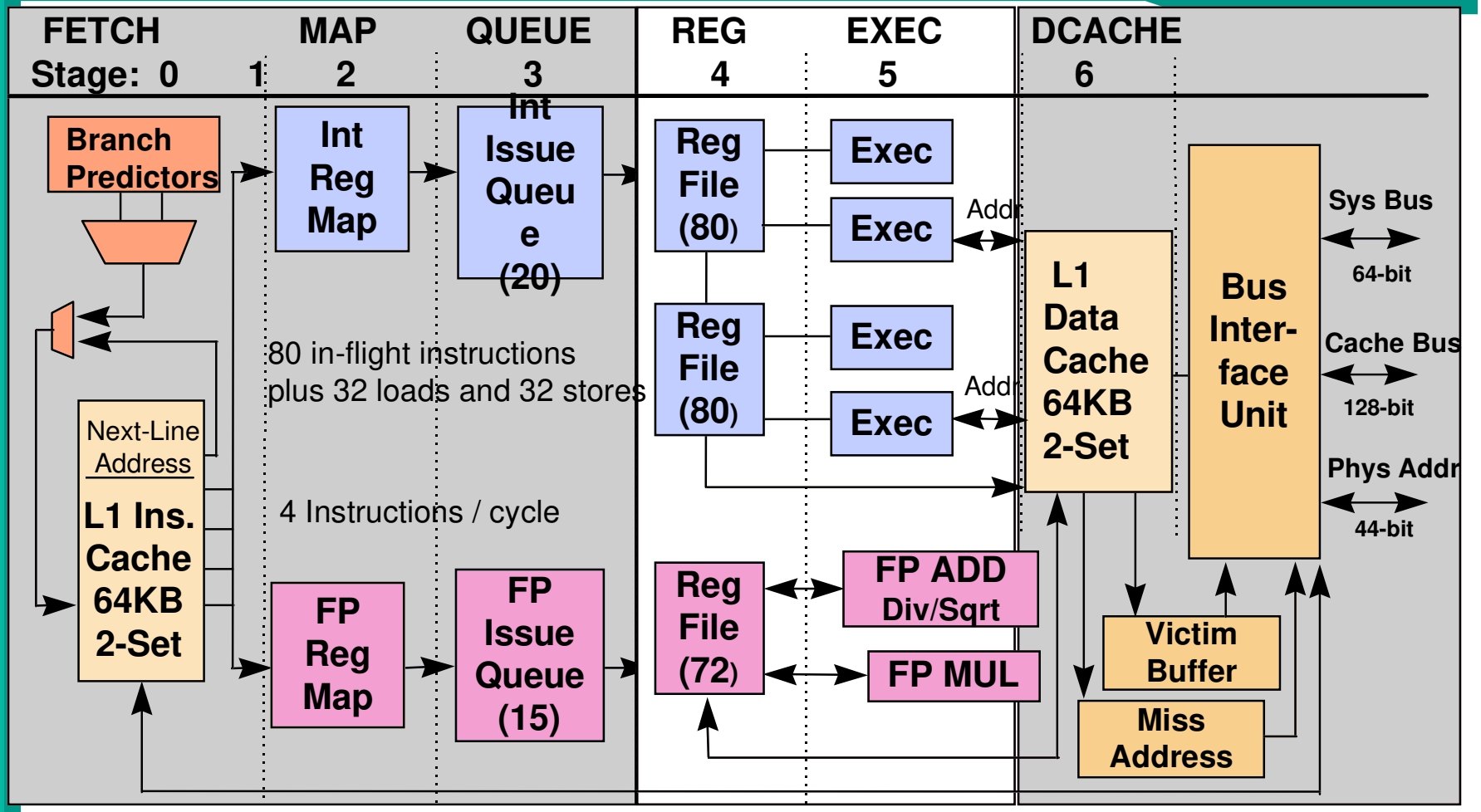
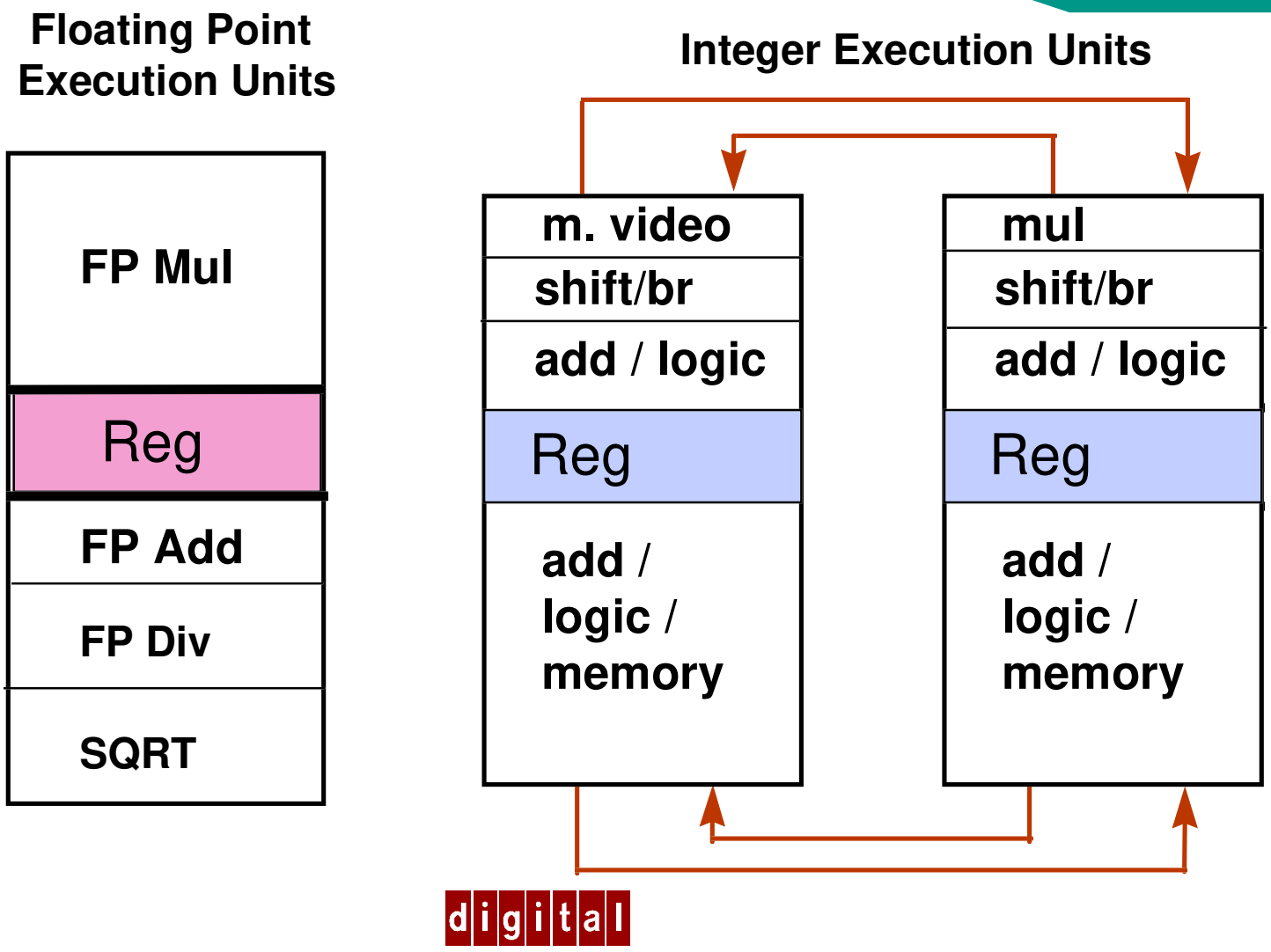
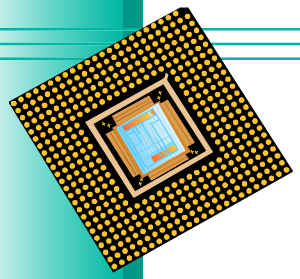


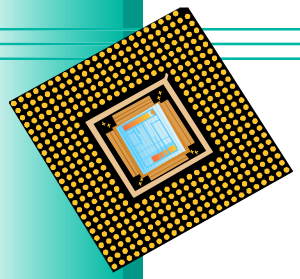
Register and Execute Stages





Floating-Point Processing

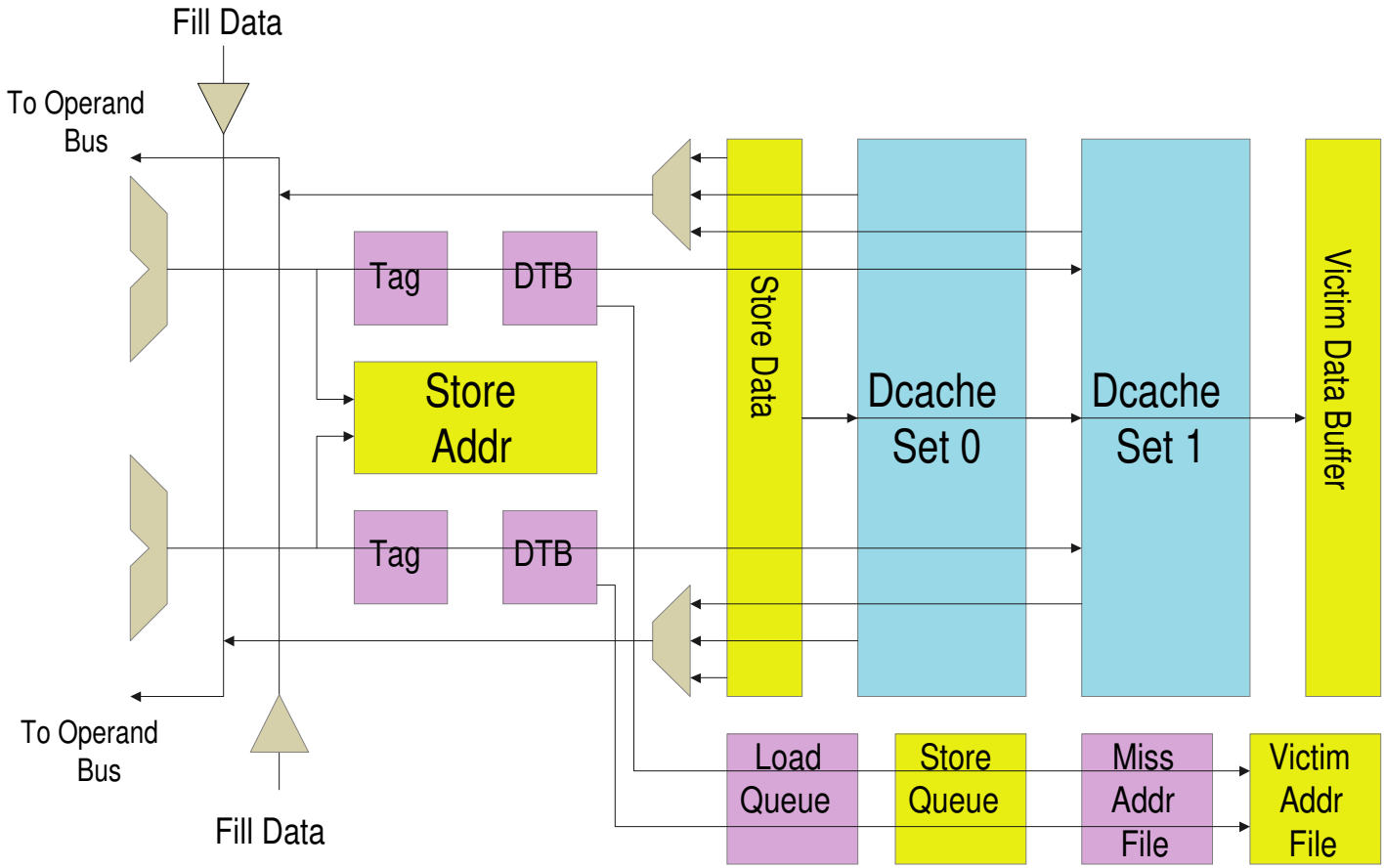
- 21264 dual-issues floating-point instructions to two independent units
  - Add / Div / Square Root unit
    - 64-bit Add: 4-cycle latency, fully pipelined
    - 64-bit IEEE Divide: 16 cycle latency
    - 64-bit Square root: 33 cycle latency
  - Multiply unit
    - 4 cycle latency, fully pipelined

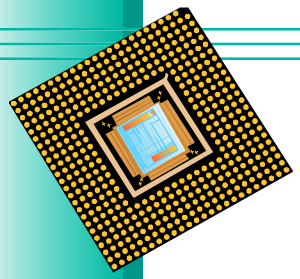


Load and Store Processing

- L1 Data Cache
  - Two loads / stores per cycle (any combination)
    - 1GHz operation: Phase pipelined - no bank conflict
    - 16 Byte read / write per cycle
- Loads and stores issue out-of-order
  - 32-entry load and store reorder buffers
  - Stores check load buffer to enforce ordering
- Cache prefetch instructions
  - Read, modify intent, non-cached, evict next

Memory Pipeline

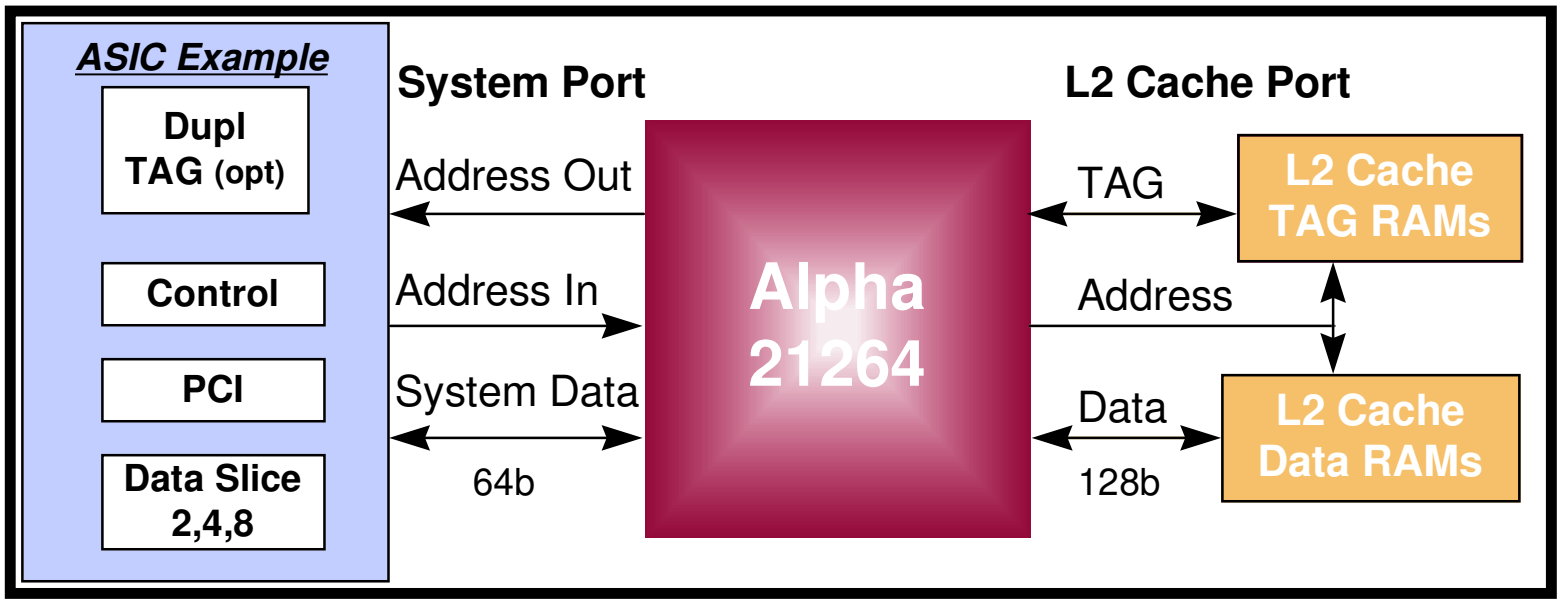




Performance-Focused Memory System

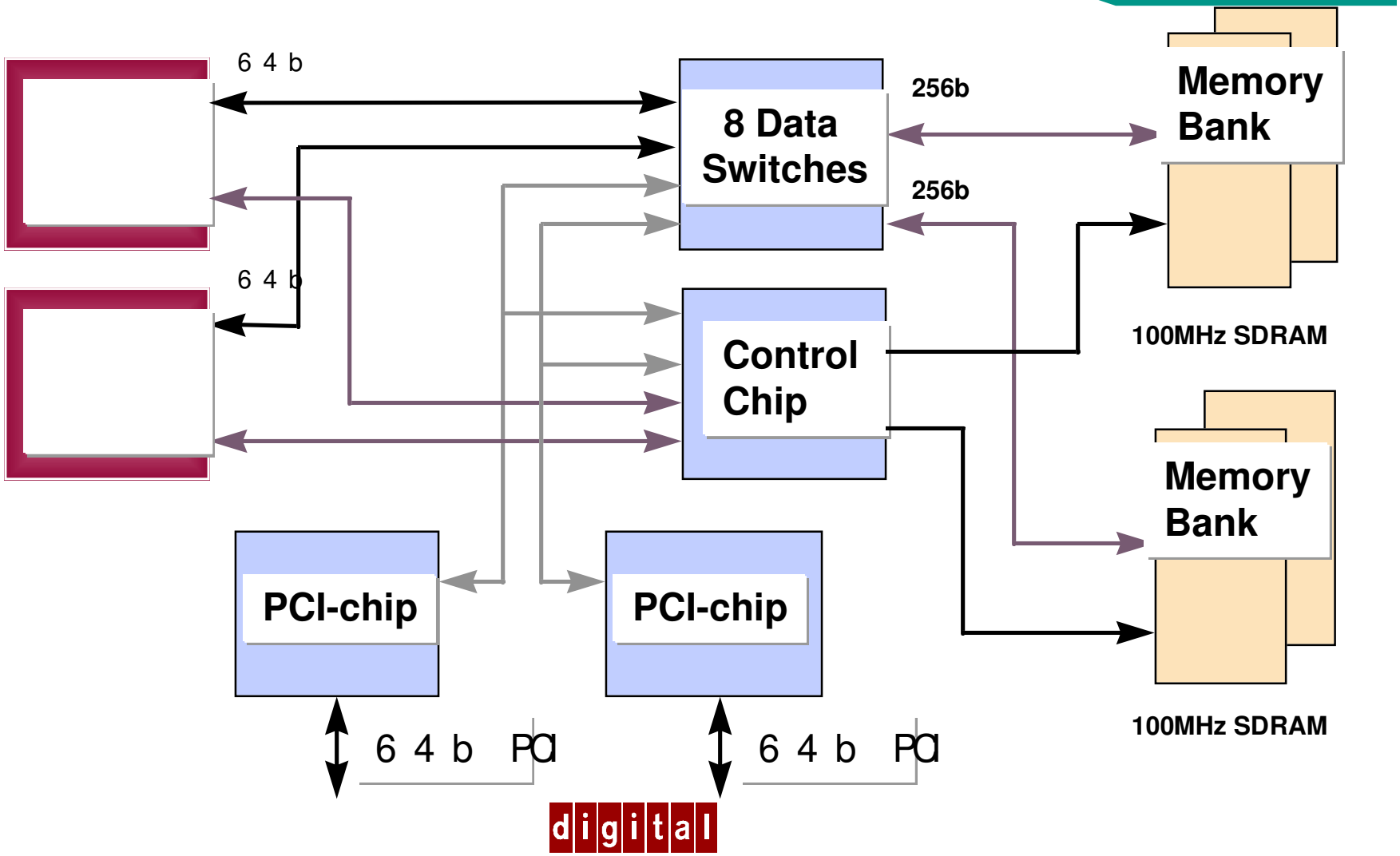
- L1 dcache: 8+ GB/s sustained bandwidth
  - 128b datapath with 3 cycle load-to-use latency
- L2 cache: 4+ GB/s sustained bandwidth
  - 128b datapath with 12 cycle load-to-use latency
- System interface: 2+ GB/s sustained bandwidth
  - 64b datapath with 80 cycle load-to-use latency
- 16 64-byte off-chip memory references
  - 8 read-misses and 8 write-backs

External Interface

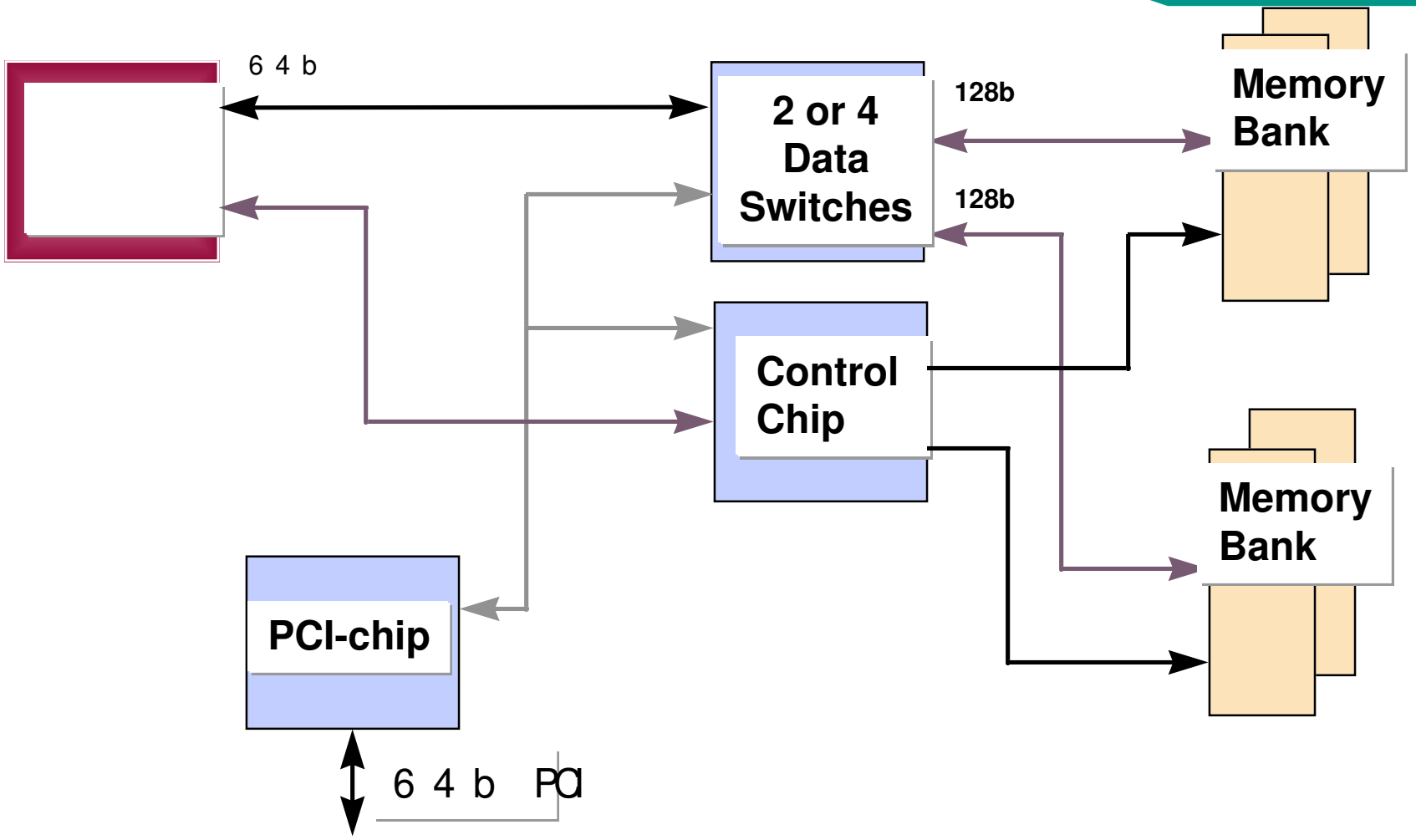


Frequency: 80 - 200 MHz Clock In	**I/O:** 2V HSTL
L2 Cache: 0 -16MB Synch Direct Mapped	**Peak Bandwidth*:***
Option 1: Reg-Reg 133 MHz BurstRAM	2.1GB/Sec
Option 2: 'RISC' 250MHz Late Write	4.0GB/Sec
Option 3: Dual Data 333MHz	5.3GB/Sec

Dual 21264 System Example



Uni 21264 System Example



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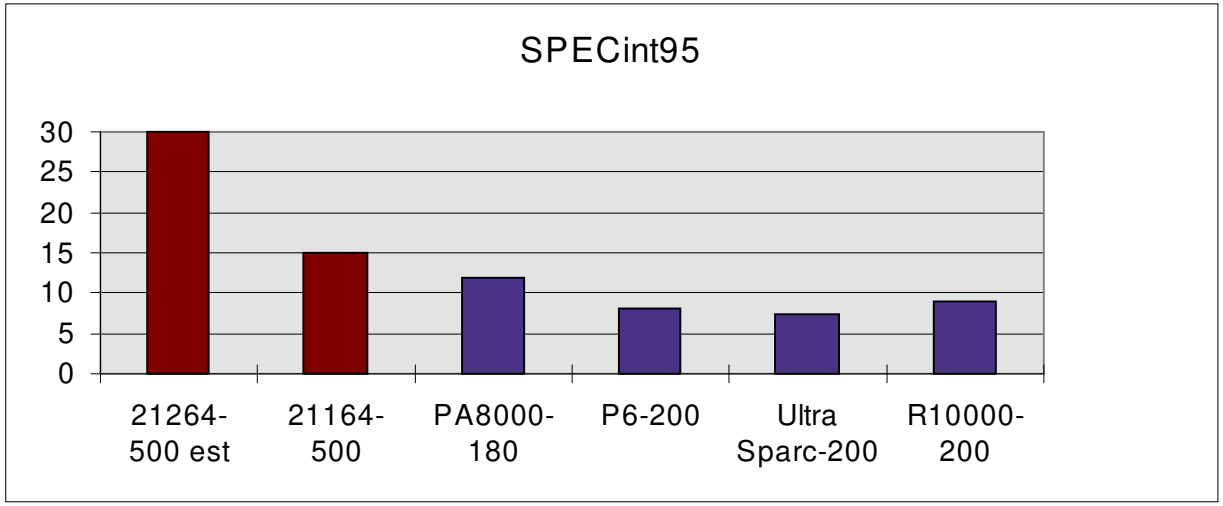
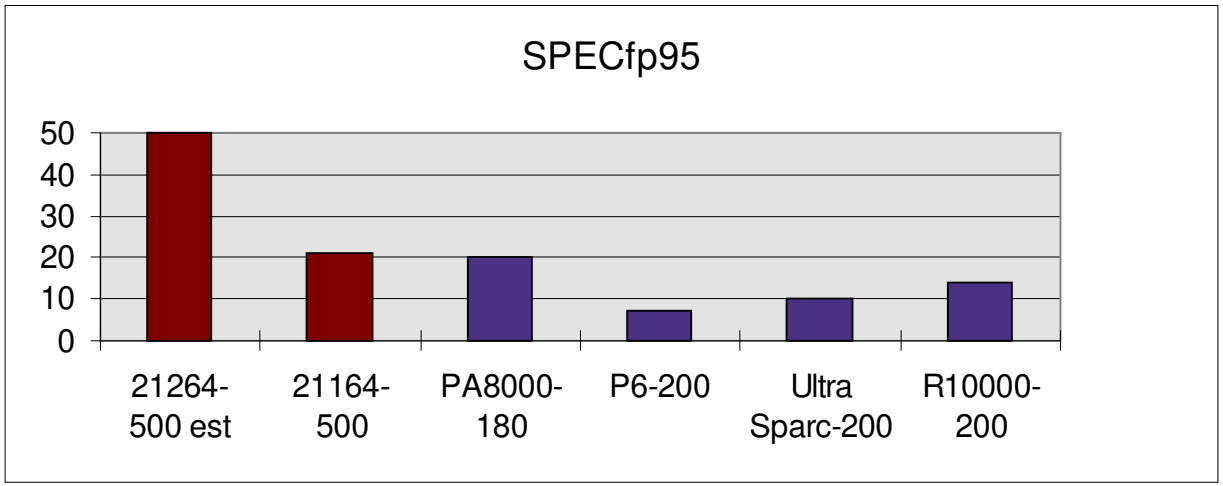
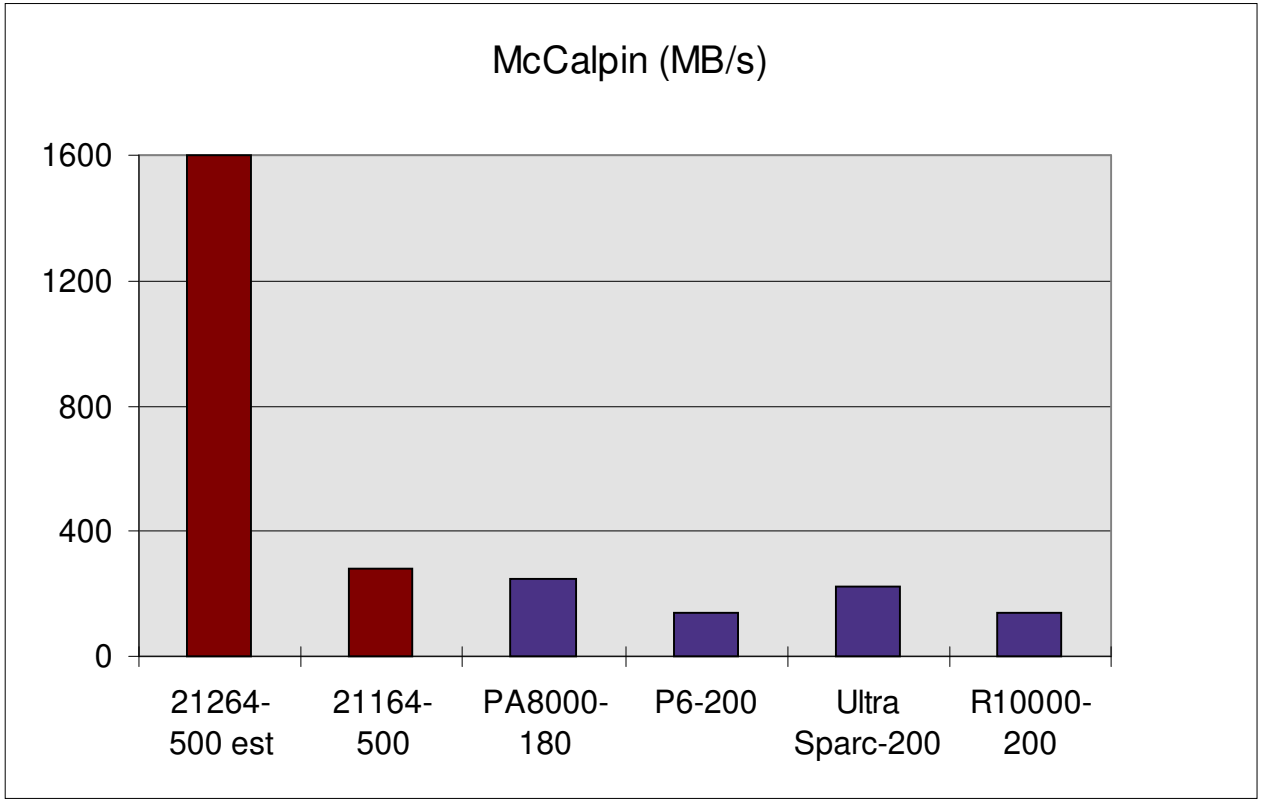
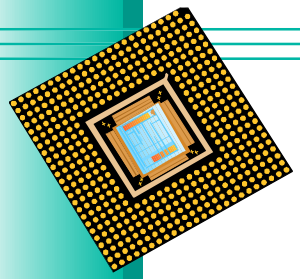
Performance Comparison: SPEC95





Performance Comparison: STREAM (McCalpin)





Summary

- 21264 will maintain Alpha's performance lead
  - 30+ SPECint95 and 50+ SPECfp95
  - Spectacular memory bandwidth
  - Out-of-order execution can be done at very high frequency