Future Technology
Dec. 4, 1996

Topics

- Semiconductor basics
- CMOS Scaling
- DRAM technology
- Flash Memory
- Atomic Scale Storage

Impact of Technology

It's the Technology, Stupid!

- Computer science has ridden the wave

Things Aren't Over Yet

- Technology will continue to progress along current growth curves
- For at least 10 more years
- Difficult technical challenges in doing so

Even Technologists Can't Beat Laws of Physics

- Quantum effects create fundamental limits as approach atomic scale
- Opportunities for new devices

Risk of Predicting the Future

Incremental Improvements Exceed Wildest Dreams

- **Silicon CMOS**
- **Magnetic disks**
- **DRAM**

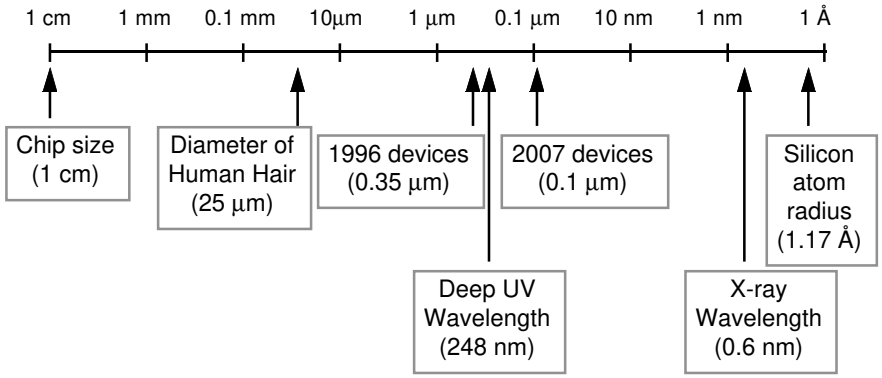
Hopes for Future Technology Never Materialize

- **Magnetic bubble memory**
- **CCD memory**
- **Gallium Arsenide**

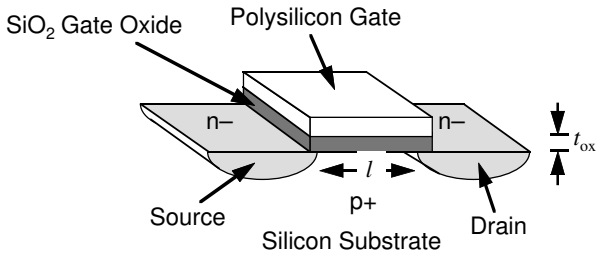
Observations

- **In this business, "incrementing" is by multiplicative factor**
- **Economies of scale favor existing technology**
- **Shifts occur due to new market forces**
  - Drive for low power due to desire for portability
  - Emphasis on networking due to WWW

Dimensions



MOS Transistor

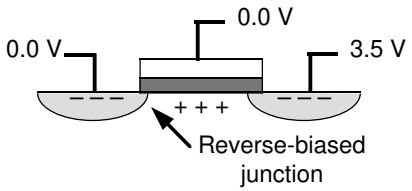


Typical Dimensions

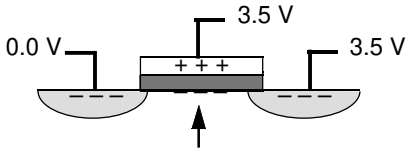
- **1996:** l **= 0.35 μm** t_{ox} **= 10 nm**
- **2007:** l **= 0.1 μm** t_{ox} **= 3.5 nm**

Transistor Operation

Off



On



I_{ds} 50 – 100 μA

Scaling to 0.1μm

- **Semiconductor Industry Association, 1992 Technology Workshop**

Year	1992	1995	1998	2001	2004	2007
Feature size	0.5	0.35	0.25	0.18	0.12	0.10
DRAM cap	16M	64M	256M	1G	4G	16G
Gates/chip	300K	800K	2M	5M	10M	20M
Chip cm^2	2.5	4.0	6.0	8.0	10.0	12.5
Intercn. levels	3	4–5	5	5–6	6	6–7
Supply Volts	5.0	3.3	2.2	2.2	1.5	1.5
I/Os	500	750	1500	2000	3500	5000
off chip MHz	60	100	175	250	350	500
on chip MHz	120	200	350	500	700	1000

Challenges Reaching 0.1 μm

Gate oxide tunneling

- **electrons jump through thin gate oxides**

Nonuniform dopant concentrations

- **< 100 dopant atoms in inversion layer**
- **Statistical variations cause varying device characteristics**

Scaling of threshold voltages

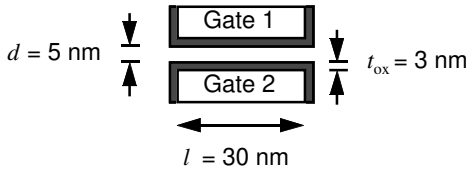
- **Difference between gate and source voltages for transistor to turn on**
- **Too low: leakage current when transistor "off"**
  - Higher standby power
- **Too high: poor performance**

Lithography

- **Reaching optical limits**
- **Alternatives (X-ray, E-beam) costly for large scale manufacturing**

Sub 0.1 μm Devices

Double Gate MOS Transistor

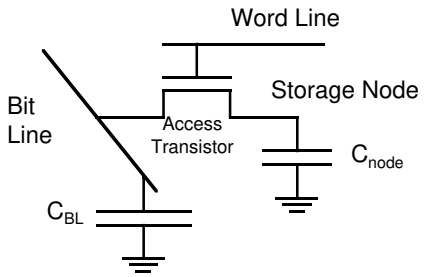


- **IBM J. R&D, Jan/Mar '95**
- **Thin channel region allows more effective shutoff**

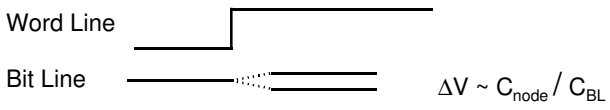
How low can you go?

- **Below 10nm (0.01 μm), quantum effects become prevalent**
- **This would be 1000 X improvement over today's areal densities**

DRAM Technology



Reading



DRAM Driving Forces

Capacity

- **4X per generation**
  - Square array of cells
- **Typical scaling**
  - Lithography dimensions 0.7X
    - » Areal density 2X
  - Cell function packing 1.5X
  - Chip area 1.33X
- **Scaling challenge**
  - Typically $C_{node} / C_{BL} = 0.1–0.2$
  - Must keep C_{node} high as shrink cell size

Retention Time

- **Typically 16–256 ms**
- **Want higher for low-power applications**

DRAM Storage Capacitor

Planar Capacitor

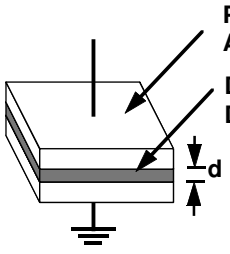
- **Up to 1Mb**
- **C decreases linearly with feature size**

Trench Capacitor

- **4–256 Mb**
- **Lining of hole in substrate**

Stacked Cell

- **> 1Gb**
- **On top of substrate**
- **Use high ε dielectric**

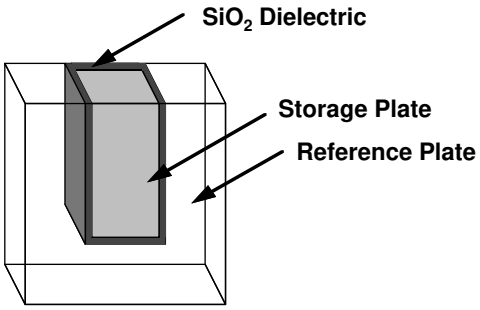


$$C = \varepsilon A/d$$

Trench Capacitor

Process

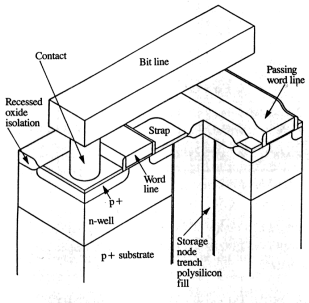
- **Etch deep hole in substrate**
  - Becomes reference plate
- **Grow oxide on walls**
  - Dielectric
- **Fill with polysilicon plug**
  - Tied to storage node



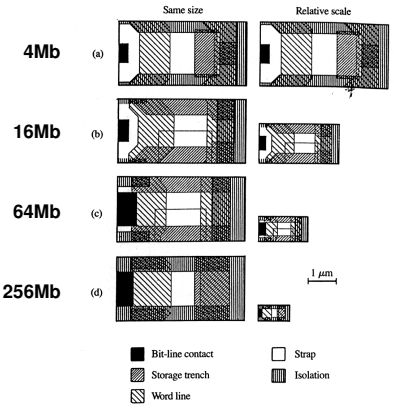
IBM DRAM Evolution

- **IBM J. R&D, Jan/Mar '95**
- **Evolution from 4 – 256 Mb**
- **256 Mb uses cell with area 0.6 μm^2**

4 Mb Cell Structure



Cell Layouts



Mitsubishi Stacked Cell DRAM

- **IEDM '95**
- **Claim suitable for 1 – 4 Gb**

Technology

- **0.14 μm process**
  - Synchrotron X-ray source
- **8 nm gate oxide**
- **0.29 μm² cell**

Storage Capacitor

- **Fabricated on top of everything else**
- **Rubidium electrodes**
- **High dielectric insulator**
  - 50X higher than SiO_2
  - 25 nm thick
- **Cell capacitance 25 femtofarads**

Cross Section of 2 Cells

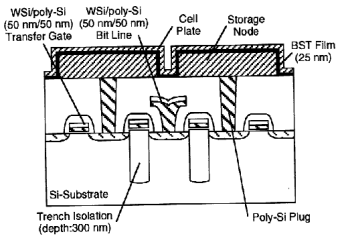


Fig. 2 Schematic cross-sectional view of DRAM memory cells with Ru/BST/Ru stacked capacitors.

Mitsubishi DRAM Pictures

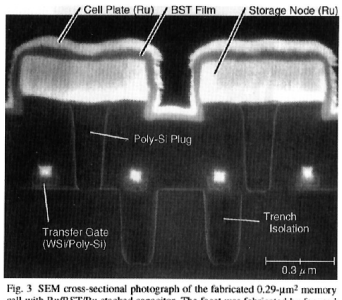


Fig. 3 SEM cross-sectional photograph of the fabricated 0.29-μm² memory cell with Ru/BST/Ru stacked capacitor. The facet was fabricated by focused ion beam etching.

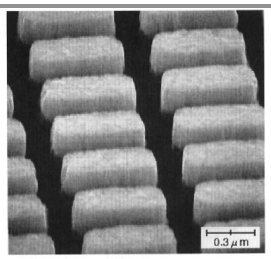


Fig. 8 SEM photograph of a Ru-metal storage node array with a projection a height of 0.2 μm.

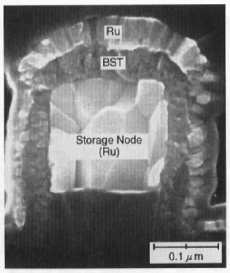


Fig. 10 SEM cross-sectional view of a Ru/BST/Ru capacitor cell. The facet shown is a cleaved facet.

Flash Memory

Characteristics

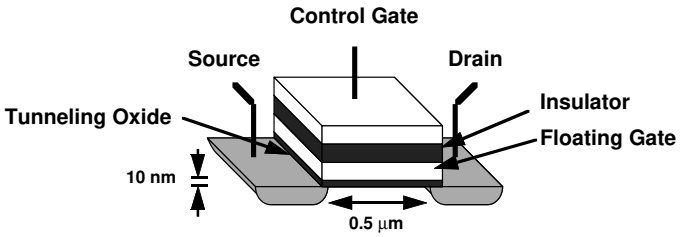
- **Retains state even when power shut off**
- **Read times comparable to DRAM**
- **Slow write times**
- **Limited endurance: ~ 100,000 read/write cycles (or less!)**

Applications

- **Semi-permanent storage**
  - Built in software, parameter RAM, font tables
  - Endurance and slow writes not an issue
- **Alternative to magnetic storage**
  - No moving parts—lower power and more rugged
  - More expensive per bit: 8 MB PCMCIA card costs $350

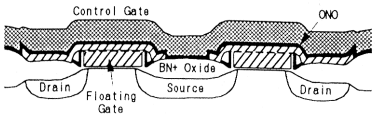
Flash Memory Cell

- **Samsung, IEDM '95**
- **Cell Size 1.6 μm^2**
  - 1.4 X denser than DRAM cell for comparable design rules
- **Simpler process**



Cross Section

- **Two Cells**
- **Common control gate**
- **Common source**



Flash Cell Writing

Based on Fowler-Nordheim Tunneling

- Electron has nonzero probability of crossing thin insulator

Erase Operation

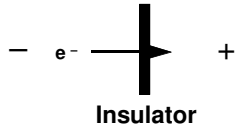
- Drive electrons into floating gate
- For entire group of cells

Program Operation

- Drive electrons out of floating gate
- For selected cell

State Retention

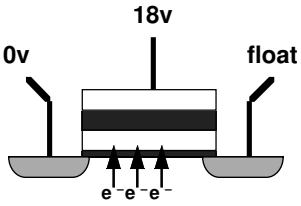
- Electrons will remain in floating gate indefinitely



Erasing Flash Cells

Erasing

- Electrons drawn into floating gate
- For entire group of cells
- ~ 400 μs



Erasing Top Row

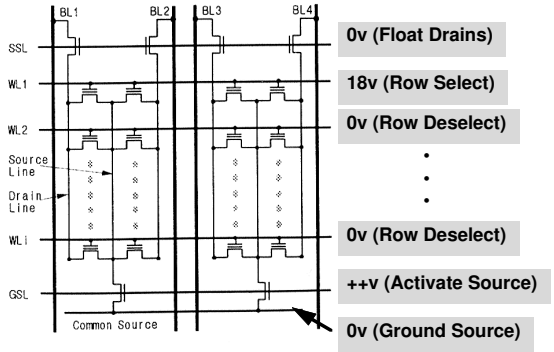
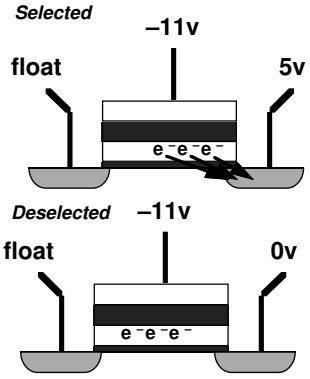


Fig. 1 Schematic diagram of the DuSNOR flash memory cell array.

Programming Flash Cell

- Electrons pushed out of floating gate
- For selected cell
- ~ 15 μs



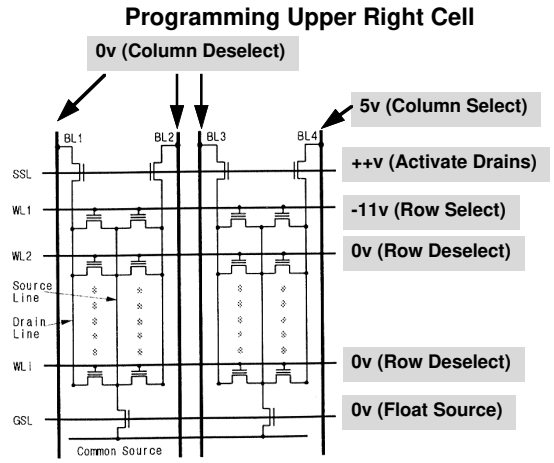
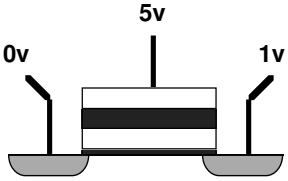


Fig. 1 Schematic diagram of the DuSNOR flash memory cell array.

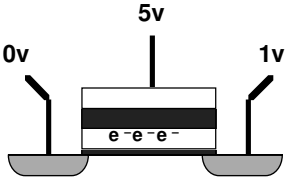
Flash Cell Reading

Programmed Cell



- Behaves like normal transistor
  - But, lower quality
- Threshold voltage = 2 v

Erased Cell



- Trapped electrons shield control gate
- Treshold voltage = 7 v

Reliability

State Retention

- **Electrons stay trapped in floating gate**
- **Good for ~ 10 years**

Endurance

- **Over many erase / program cycles, electrons become trapped in tunneling oxide**
  - OK for 100,000 cycles
- **Causes threshold voltage for programmed cell to rise**

Micro Disks

Motivation

- **Current disk drives give high capacity but poor access times**
- **Mechanical components limit reliability and consume power**

Microelectronic Mechanical Systems (MEMS)

- **Fabricate mechanical devices using VLSI processing technology**
- **Currently used for miniaturized sensors and actuators**

Silicon Disk

- **Proposed technology for high density storage**
- **Goal is to get 100 Gb in 1cm^2**
  - 3 nm X 3 nm bit storage
  - 1 % of surface used for bit storage
    - » Rest for electronics and actuators

Storage Array

- **Probe tip moves over 32 X 32 array of bits**
- **Arm controlled by electrostatic actuator**
- **Uses tunneling to read/write bits**