15-740/18-740 Computer Architecture
Fall 2009 Schedule

Table 1: 15-740/18-740, Fall 2009, Tentative Schedule.

Class	Date	Day	Topic	Reading	Assignments
1	9/8	Tue	Performance & Technology	H&P Ch. 1	
2	9/9	Wed	x86 Programming	H&P App.. J.3	
3	9/10	Thu	RISC vs. CISC Instruction Sets	H&P App. B & J	
4	9/15	Tue	The Memory Hierarchy	H&P Ch. 5	#1 Out
5	9/16	Wed	Intro to Parallel Architecture	H&P Ch. 4.1,CSG Ch. 1	
6	9/17	Thu	Parallel Programming I	CSG Ch. 2	
	9/22	Tue	*No Class: Gates Hall Dedication*		
7	9/23	Wed	Parallel Programming II	CSG Ch. 3 & 4	
	9/24	Thu	*No Class: G-20 Event at Phipps*		
8	9/29	Tue	Cache Coherence I	H&P Ch. 4.2-4.3, CSG Ch. 5	#1 Due, #2 Out
9	9/30	Wed	Cache Coherence II	H&P Ch. 4.4, CSG Ch. 5	
10	10/1	Thu	Cache Coherence III	H&P Ch. 4.4, CSG Ch. 5	
11	10/6	Tue	Memory Consistency	H&P Ch. 4.6, CSG Ch. 6	
12	10/7	Wed	TLS and Transactional Memory	Handouts	
	10/8	Thu	**Exam I**		
13	10/13	Tue	*Recent Research on Architecture I*	Handouts	
14	10/14	Wed	*Recent Research on Architecture II*	Handouts	#2 Due
15	10/15	Thu	*Recent Research on Architecture III*	Handouts	
16	10/20	Tue	Synchronization	H&P Ch. 4.5, CSG Ch. 5	
17	10/21	Wed	Interconnection Networks	H&P App. E, CSG Ch. 10	Project Proposal
18	10/22	Thu	Virtual Memory	H&P Ch. 5.4, App. C.4-C.5	
19	10/27	Tue	Basic Pipelining	H&P Ch. 2.1, App. A.1	
20	10/28	Wed	Pipelining Hazards	H&P App. A.2-A.6	
21	10/29	Thu	Instruction-Level Parallelism	H&P Ch. 2.2-2.10	
	11/5	Thu	**Exam II**		
	11/17	Tue			Project Milestone
	12/1	Tue			Project Due
	12/3	Thu	*Project Poster Session*		