NOTE: the following paper is good background reading for these first two discussion topics, but it is not something that you should explicitly cover: Austen McDonald, JaeWoong Chung, Brian D. Carlstrom, Chi Cao Minh, Hassan Chafi, Christos Kozyrakis, and Kunle Olukotun. “Architectural Semantics for Practical Transactional Memory,” in Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA), June 2006.

Transactional Memory: Supporting Large Transactions


Transactional Memory: Hybrid Hardware/Software Approaches


Thread-Level Speculation


Load Imbalance in Chip Multiprocessors


Cache Organization and Performance for Chip Multiprocessors


On-Chip Interconnects


Cache Coherence


Memory Consistency


Data Parallelism: Streams and Graphics Processors


Recording Inter-Thread Data Dependencies for Deterministic Replay


Dynamic Checking of Program Invariants


Optimizing Power and Heat


