15-740 Computer Architecture, Fall 2007
Papers for In-Class Discussions

NOTE: the following paper is good background reading for these first two discussion topics, but it is not something that you should explicitly cover: Austen McDonald, JaeWoong Chung, Brian D. Carlstrom, Chi Cao Minh, Hassan Chafi, Christos Kozyrakis, and Kunle Olukotun. *"Architectural Semantics for Practical Transactional Memory,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

Transactional Memory: Supporting Large Transactions

- Ravi Rajwar, Maurice Herlihy, and Konrad Lai. *"Virtualizing Transactional Memory,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Wei Chuang, Satish Narayanasamy, Ganesh Venkatesh, Jack Sampson, Michael Van Biesbrouck, Gilles Pokam, Osvaldo Colavin and Brad Calder. *"Unbounded Page-Based Transactional Memory,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- JaeWoong Chung, Chi Cao Minh, Austen McDonald, Travis Skare, Hassan Chafi, Brian D Carlstrom, Christos Kozyrakis and Kunle Olukotun. *"Tradeoffs in Transactional Memory Virtualizations,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Colin Blundell, Joe Devietti, E. Christopher Lewis, and Milo M. K. Martin. *"Making the Fast Case Common and the Uncommon Case Simple in Unbounded Transactional Memory,"*, in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Transactional Memory: Hybrid Hardware/Software Approaches

- Peter Damron, Alexandra Fedorova, Yossi Lev, Victor Luchangco, Mark Moir and Dan Nussbaum. *"Hybrid Transactional Memory,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Chi Cao Minh, Martin Trautmann, JaeWoong Chung, Austen McDonald, Nathan Bronson, Jared Casper, Christos Kozyrakis, and Kunle Olukotun. *"An Effective Hybrid Transactional Memory System with Strong Isolation Guarantees,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Arrvindh Shriraman, Michael F Spear, Hemayet Hossain, Virendra J Marathe, Sandhya Dwarkadas, and Michael L Scott. *"An Integrated Hardware-Software Approach to Flexible Transactional Memory,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Thread-Level Speculation

- Christopher B. Colohan, Anastassia Ailamaki, J. Gregory Steffan, and Todd C. Mowry. *"Tolerating Dependences Between Large Speculative Threads Via Sub-Threads,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

- Luis Ceze, James Tuck, Calin Cascaval, and Josep Torrellas. *"Bulk Disambiguation of Speculative Threads in Multiprocessors,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

Load Imbalance in Chip Multiprocessors

- Saisanthosh Balakrishnan, Ravi Rajwar, Mike Upton, and Konrad Lai. *"The Impact of Performance Asymmetry in Emerging Multicore Architectures,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Sanjeev Kumar, Christopher J Hughes, and Anthony Nguyen. *"Carbon: Architectural Support for Fine-Grained Parallelism on Chip Multiprocessors,"*, in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Cache Organization and Performance for Chip Multiprocessors

- Jacob Leverich, Hideho Arakida, Alex Solomatnikov, Amin Firoozshahian, Mark Horowitz, and Christos Kozyrakis. *"Comparing Memory Systems for Chip Multiprocessors,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Evan Speight, Hazim Shafi, Lixin Zhang, and Ram Rajamony. *"Adaptive Mechanisms and Policies for Managing Cache Hierarchies in Chip Multiprocessors,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Jichuan Chang and Gurindar S. Sohi. *"Cooperative Caching for Chip Multiprocessors,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

On-Chip Interconnects

- Rakesh Kumar, Victor Zyuban, and Dean M. Tullsen. *"Interconnections in Multi-Core Architectures: Understanding Mechanisms, Overheads and Scaling,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Naveen Muralimanohar and Rajeev Balasubramonian. *"Interconnect Design Considerations for Large NUCA Caches,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Cache Coherence

- Andreas Moshovos. *"RegionScout: Exploiting Coarse Grain Sharing in Snoop-Based Coherence,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Jason F. Cantin, Mikko H. Lipasti, and James E. Smith. *"Improving Multiprocessor Performance with Coarse-Grain Coherence Tracking,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Liqun Cheng, Naveen Muralimanohar, Karthik Ramani, Rajeev Balasubramonian, and John B. Carter. *"Interconnect-Aware Coherence Protocols for Chip Multiprocessors,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

Memory Consistency

- Arvind and Jan Willem Maessen. *"Memory Model = Instruction Reordering + Store Atomicity,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Christoph von Praun, Harold W. Cain, Jong-Deok Choi, and Kyung Dong Ryu. *"Conditional Memory Ordering,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Thomas F Wenisch, Anastasia Ailamaki, Babak Falsafi, and Andreas Moshovos. *"Mechanisms for Store-wait-free Multiprocessors,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

- Luis Ceze, James Tuck, Pablo Montesinos, and Josep Torrellas. *"BulkSC: Bulk Enforcement of Sequential Consistency,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Data Parallelism: Streams and Graphics Processors

- Michael I. Gordon, William Thies and Saman Amarasinghe. *"Exploiting Coarse-Grained Task, Data, and Pipeline Parallelism in Stream Processors,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- David Tarditi, Sidd Puri and Jose Oglesby. *"Accelerator: Using Data-Parallelism to Program GPUs for General-Purpose Uses,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.

Recording Inter-Thread Data Dependencies for Deterministic Replay

- Min Xu, Rastislav Bodik, and Mark D. Hill. *"A 'Flight Data Recorder' for Enabling Full-system Multiprocessor Deterministic Replay,"* in *Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA)*, June 2003.
- Min Xu, Rastislav Bodik and Mark Hill. *"A Regulated Transitive Reduction for Longer Memory Race Recording,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Satish Narayanasamy, Gilles Pokam, and Brad Calder. *"BugNet: Continuously Recording Program Execution for Deterministic Replay Debugging,"* in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Satish Narayanasamy, Cristiano Pereira and Brad Calder. *"Recording Shared Memory Dependencies Using Strata,"* in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.

Dynamic Checking of Program Invariants

- Shan Lu, Joseph Tucek, Feng Qin and Yuanyuan Zhou. *"AVIO: Detecting Atomicity Violations via Access Interleaving Invariants,"*, in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Michael Dalton, Hari Kannan, and Christos Kozyrakis. *"Raksha: A Flexible Information Flow Architecture for Software Security,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Optimizing Power and Heat

- James Donald and Margaret Martonosi. *"Techniques for Multicore Thermal Management: Classification and New Exploration,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Bruno Diniz, Dorgival Guedes, Wagner Meira Jr., and Ricardo Bianchini. *"Limiting the Power Consumption of Main Memory,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Parthasarathy Ranganathan, Phil Leech, David Irwin, and Jeff Chase. *"Ensemble-level Power Management for Dense Blade Servers,"* in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Xiaobo Fan, Wolf-Dietrich Weber, and Luiz Andre Barroso. *"Power Provisioning for a Warehouse-sized Computer,"* in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.