

15-740 Computer Architecture, Fall 2007

Schedule for In-Class Discussions

Day 1: *Tuesday, October 9, 2007*

Transactional Memory: Supporting Large Transactions: Conventional designs for hardware-supported transactional memory can only handle transactions of a limited size: how can we extend this support to larger transactions?

- Ravi Rajwar, Maurice Herlihy, and Konrad Lai. “*Virtualizing Transactional Memory*,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Wei Chuang, Satish Narayanasamy, Ganesh Venkatesh, Jack Sampson, Michael Van Biesbrouck, Gilles Pokam, Osvaldo Colavin and Brad Calder. “*Unbounded Page-Based Transactional Memory*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- JaeWoong Chung, Chi Cao Minh, Austen McDonald, Travis Skare, Hassan Chafi, Brian D Carlstrom, Christos Kozyrakis and Kunle Olukotun. “*Tradeoffs in Transactional Memory Virtualizations*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Colin Blundell, Joe Devietti, E. Christopher Lewis, and Milo M. K. Martin. “*Making the Fast Case Common and the Uncommon Case Simple in Unbounded Transactional Memory*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Transactional Memory: Hybrid Hardware/Software Approaches: How can we combine software- and hardware-based transactional memory to get the best of both worlds?

- Peter Damron, Alexandra Fedorova, Yossi Lev, Victor Luchangco, Mark Moir and Dan Nussbaum. “*Hybrid Transactional Memory*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Chi Cao Minh, Martin Trautmann, JaeWoong Chung, Austen McDonald, Nathan Bronson, Jared Casper, Christos Kozyrakis, and Kunle Olukotun. “*An Effective Hybrid Transactional Memory System with Strong Isolation Guarantees*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Arrvindh Shriraman, Michael F Spear, Hemayet Hossain, Virendra J Marathe, Sandhya Dwarkadas, and Michael L Scott. “*An Integrated Hardware-Software Approach to Flexible Transactional Memory*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Thread-Level Speculation: Recent work on optimistically exploiting thread-level parallelism.

- Christopher B. Colohan, Anastassia Ailamaki, J. Gregory Steffan, and Todd C. Mowry. “*Tolerating Dependences Between Large Speculative Threads Via Sub-Threads*,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Luis Ceze, James Tuck, Calin Cascaval, and Josep Torrellas. “*Bulk Disambiguation of Speculative Threads in Multiprocessors*,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

Load Imbalance in Chip Multiprocessors: What is the impact of asymmetry in a CMP, and how can we efficiently support dynamic scheduling?

- Saisanthosh Balakrishnan, Ravi Rajwar, Mike Upton, and Konrad Lai. “*The Impact of Performance Asymmetry in Emerging Multicore Architectures*,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Sanjeev Kumar, Christopher J Hughes, and Anthony Nguyen. “*Carbon: Architectural Support for Fine-Grained Parallelism on Chip Multiprocessors*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Table 1: Day 1 Discussion Leaders

Topic	Time Slot	Discussion Leaders
TM: Large Transactions	12:00-12:20	Vijay Vasudevan Hetu Kamichetty
TM: Hybrid HW/SW Approaches	12:20-12:40	Paul Zagieboylo Severin Hacker
Thread-Level Speculation	12:40-1:00	Xi Liu Lei Li
Load Imbalance	1:00-1:20	Fan Guo Kyung-Ah Sohn

Day 2: Thursday, October 11, 2007

Cache Organization and Performance for Chip Multiprocessors: How should the design of the cache hierarchy change for a chip multiprocessor?

- Jacob Leverich, Hideho Arakida, Alex Solomatnikov, Amin Firoozshahian, Mark Horowitz, and Christos Kozyrakis. “Comparing Memory Systems for Chip Multiprocessors,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Evan Speight, Hazim Shafi, Lixin Zhang, and Ram Rajamony. “Adaptive Mechanisms and Policies for Managing Cache Hierarchies in Chip Multiprocessors,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Jichuan Chang and Gurindar S. Sohi. “Cooperative Caching for Chip Multiprocessors,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

On-Chip Interconnects: How should the on-chip interconnect be designed for a chip multiprocessor, and how does this design interact with the on-chip cache hierarchy?

- Rakesh Kumar, Victor Zyuban, and Dean M. Tullsen. “Interconnections in Multi-Core Architectures: Understanding Mechanisms, Overheads and Scaling,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Naveen Muralimanohar and Rajeev Balasubramonian. “Interconnect Design Considerations for Large NUCA Caches,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Cache Coherence: Recent innovations in cache coherence protocols.

- Andreas Moshovos. “RegionScout: Exploiting Coarse Grain Sharing in Snoop-Based Coherence,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Jason F. Cantin, Mikko H. Lipasti, and James E. Smith. “Improving Multiprocessor Performance with Coarse-Grain Coherence Tracking,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Liquan Cheng, Naveen Muralimanohar, Karthik Ramani, Rajeev Balasubramonian, and John B. Carter. “Interconnect-Aware Coherence Protocols for Chip Multiprocessors,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.

Memory Consistency: Recent innovations in supporting memory consistency models.

- Arvind and Jan Willem Maessen. “Memory Model = Instruction Reordering + Store Atomicity,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Christoph von Praun, Harold W. Cain, Jong-Deok Choi, and Kyung Dong Ryu. “Conditional Memory Ordering,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Thomas F Wenisch, Anastasia Ailamaki, Babak Falsafi, and Andreas Moshovos. “Mechanisms for Store-wait-free Multiprocessors,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Luis Ceze, James Tuck, Pablo Montesinos, and Josep Torrellas. “BulkSC: Bulk Enforcement of Sequential Consistency,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Table 2: Day 2 Discussion Leaders

Topic	Time Slot	Discussion Leaders
Caches for CMPs	12:00-12:20	Wittawat Tantisiriroj Eric Blais
On-Chip Interconnects	12:20-12:40	Michael Papamichael Hormoz Zarnini
Cache Coherence	12:40-1:00	Carsten Varming Michael Ashley-Rollman
Memory Consistency	1:00-1:20	Shobhit Dayal Dilip Kumar Uppugandla

Day 3: *Tuesday, October 16, 2007*

Data Parallelism: Streams and Graphics Processors: Interesting ways to exploit data parallelism for stream programs and for GPUs.

- Michael I. Gordon, William Thies and Saman Amarasinghe. “*Exploiting Coarse-Grained Task, Data, and Pipeline Parallelism in Stream Processors*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- David Tarditi, Sidd Puri and Jose Oglesby. “*Accelerator: Using Data-Parallelism to Program GPUs for General-Purpose Uses*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.

Recording Inter-Thread Data Dependencies for Deterministic Replay: To support debugging of parallel programs, we need to be able to reconstruct inter-thread data dependencies. How do we do this efficiently?

- Min Xu, Rastislav Bodik, and Mark D. Hill. “*A ‘Flight Data Recorder’ for Enabling Full-system Multiprocessor Deterministic Replay*,” in *Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA)*, June 2003.
- Min Xu, Rastislav Bodik and Mark Hill. “*A Regulated Transitive Reduction for Longer Memory Race Recording*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
- Satish Narayanasamy, Gilles Pokam, and Brad Calder. “*BugNet: Continuously Recording Program Execution for Deterministic Replay Debugging*,” in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.
- Satish Narayanasamy, Cristiano Pereira and Brad Calder. “*Recording Shared Memory Dependencies Using Strata*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.

Dynamic Checking of Program Invariants: Techniques for monitoring programs as they execute to check for bugs and security problems.

- Shan Lu, Joseph Tucek, Feng Qin and Yuanyuan Zhou. “*AVIO: Detecting Atomicity Violations via Access Interleaving Invariants*,” in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.

- Michael Dalton, Hari Kannan, and Christos Kozyrakis. “*Raksha: A Flexible Information Flow Architecture for Software Security*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Optimizing Power and Heat: Power and thermal issues are major constraints on hardware technology these days. What can we do to improve power efficiency?

- James Donald and Margaret Martonosi. “*Techniques for Multicore Thermal Management: Classification and New Exploration*,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Bruno Diniz, Dorgival Guedes, Wagner Meira Jr., and Ricardo Bianchini. “*Limiting the Power Consumption of Main Memory*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.
- Parthasarathy Ranganathan, Phil Leech, David Irwin, and Jeff Chase. “*Ensemble-level Power Management for Dense Blade Servers*,” in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2006.
- Xiaobo Fan, Wolf-Dietrich Weber, and Luiz Andre Barroso. “*Power Provisioning for a Warehouse-sized Computer*,” in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

Table 3: Day 3 Discussion Leaders

Topic	Time Slot	Discussion Leaders
Data Parallelism	12:00-12:20	Yongjun Jeon Wei Yu
Deterministic Replay	12:20-12:40	Jason Franklin Michelle Goodstein
Dynamic Checking	12:40-1:00	Pongsin Poosankam Amar Phanishayee
Optimizing Power	1:00-1:20	Karthik Lakshmanan Wenjie Fu