Lect 07
Answers

Direct Mapped Cache Simulation

t=1	s=2	b=1
x	xx	x

N=16 byte addresses B=2 bytes/block S=4 sets E=1 entry/set

Address trace (reads):

0 [0000] 1 [0001] 13 [1101] 8 [1000] 0 [0000]

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

0 [0000] (miss)

(1)

v	tag	data
1	0	m[1] m[0]

13 [1101] (miss)

(2)

v	tag	data
1	0	m[1] m[0]
1	1	m[13] m[12]

8 [1000] (miss)

(3)

v	tag	data
1	1	m[9] m[8]

0 [0000] (miss)

(4)

v	tag	data
1	0	m[1] m[8]
1	1	m[13] m[12]

2-Way Set Associative Simulation

t=2	s=1	b=1
xx	x	x

N=16 addresses B=2 bytes/line S=2 sets E=2 entries/set

Address trace (reads):

0 [0000] 1 [0001] 13 [1101] 8 [1000] 0 [0000]

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

v	tag	data	v	tag	data
1	00	m[1] m[0]			

0 (miss)

v	tag	data	v	tag	data
1	00	m[1] m[0]	1	11	m[13] m[12]

13 (miss)

v	tag	data	v	tag	data
1	10	m[9] m[8]	1	11	m[13] m[12]

8 (miss)
(LRU replacement)

v	tag	data	v	tag	data
1	10	m[9] m[8]	1	00	m[1] m[0]

0 (miss)
(LRU replacement)

Fully Associative Cache Simulation

N=16 addresses B=2 bytes/line S=1 sets E=4 entries/set
Address trace (reads):
0 [0000] 1 [0001] 13 [1101] 8 [1000] 0 [0000]

t=3	s=0	b=1
xxx		x

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

0 (miss)

(1)

v	tag	data
1	00	m[1] m[0]

set ø

13 (miss)

(2)

v	tag	data
1	000	m[1] m[0]
1	110	m[13] m[12]

8 (miss)

(3)

v	tag	data
1	000	m[1] m[0]
1	110	m[13] m[12]
1	100	m[9] m[8]