CS 347 Course Logistics

Randal E. Bryant
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Topics

• instructors
• textbook
• grading
• recitations
• schedule

URL: http://www.cs.cmu.edu/afs/cs/academic/class/15347-s98/www/home.html
Newsgroup: cmu.cs.class.cs347
Teaching staff

Instructors
– Prof. Randy Bryant (Mon 3-4, 7128 Wean)
– Prof. Todd Mowry (Fri 10-11, 8123 Wean)

TA’s
– Herb Derby (Tues 1:30-2:30, 7130 Wean)
– Jason Flinn (Wed 10:30-11:30, 8208 Wean)
– Miroslav Velev (Thurs 2-3, 2134 Hammerschlag)

Course secretary
– Joan Maddamma (7121 Wean)

These are the nominal office hours. Come talk to us anytime!
(Or send email)
Textbook

J. L. Hennessy and D. Patterson,

- *Computer Organization and Design: The Hardware / Software Interface*,
- *Second Edition*

Relation to Course Material

- Solid coverage of basics
- We will supplement heavily

Platform Issues

- Book based on MIPS instruction set architecture
- We will be using Alpha
- Conceptually very similar
  - Both based on RISC philosophy
Grading

Tests (50%)
• Two in class exams (12.5% each)
• Final (25%)

Assignments (50%)
• 4 homeworks (~1 week, 3-5% each)
• 3 labs (~2 weeks, 8-12% each)
• May collaborate in groups of up to three

Grading Characteristics
• Assignment scores tend to be high
  – Serious handicap if don’t hand one in
• Tests have big bearing on letter grade
  – Wider range of scores
  – Only chance for us to evaluate individual performance
Recitations

Recitation Coverage
• Supplement lecture material
• Useful information regarding labs and assignments
• Talk about important tools
  – performance analysis, scripting languages

Attendance
• Not recorded
• Highly recommended
# Schedule: First Part

<table>
<thead>
<tr>
<th>Class</th>
<th>Date</th>
<th>Topic</th>
<th>Reading</th>
<th>Asst</th>
<th>Lect</th>
</tr>
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<tbody>
<tr>
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<td>2.1--3</td>
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<td>Integer arithmetic</td>
<td>4.1--7</td>
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<td>H1 Due, H2 Out</td>
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<td>02/05</td>
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<td>02/10</td>
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<td>I/O, Storage</td>
<td>8.1--10</td>
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<td>02/17</td>
<td>Exam #1</td>
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</table>
First Part Highlights

Primary Coverage

• Arithmetic
• Memory hierarchy

Assignments

• H1: Performance measurement
• H2: Arithmetic
• L1: Cache simulator
  – Evaluate how different cache designs would perform on actual programs
# Schedule: Second Part

<table>
<thead>
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<th>Lect</th>
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Second Part Highlights

Coverage

- Machine-level programming
- Optimizing code performance
  - Based on properties of compilers, CPUs, memory system
- CPU implementation

Assignments

- H3: Machine level programming
- L2: Program optimization
  - Hands-on experience with important programming skill
## Schedule: Third Part

<table>
<thead>
<tr>
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Third Part Highlights

Coverage

• Rest of CPU design
• Characteristics and architectural implications of multimedia computing
• Networking
• Parallel processing

Assignments

• L3 Pipeline simulator
  – Simulate pipelined Alpha implementation
  – Develop comprehensive test suite
  – Largest assignment of term
• H4 Multimedia Computing
Platform

Digital Alpha 21164
• One of the fastest processors available
  – 460 Mhz, lots of horsepower
• Nice instruction set
  – Easy to learn & implement simulator
• Excellent performance tuning tools

The Catch
• Not available yet
• Have arranged course so that we don’t need until mid-February