

15-213
"The course that gives CMU its Zip!"
Machine-Level Programming I:
Introduction
Jan. 22, 2008

Topics

- Assembly Programmer's Execution Model
- Accessing Information
 - Registers
 - Memory
- Arithmetic operations

class04.ppt
15-213, S08

Synchronization

Lab 1

- Time roughly 50% done
- Many have started early and made good progress
 - Good
- Warning to others...
 - This isn't the same kind of thing you've done before
 - Please don't leave it to the last minute

Fish-machine log-ins

- Please let us know (staff mailing list) if you can't log in to any machine

2
15-213, S08

Outline

Some computer languages

- Whitespace
- Intercal
- M

Some discussion of x86, x86-64

- Warning: Chapter 3 doesn't compress well
 - 100 pages of discussion about machine language
 - ... after 75 pages of data representation in Chapter 2
- Please plan to spend time reading the text!

3
15-213, S08

A Whitespace Program

"Count from 1 to 10" (partial listing)

Features of Whitespace

- Only space, tab, and line-feed encode program statements
- All other characters (A-Z, a-z, 0-9, etc.) encode comments
- Simple stack-based language

4
15-213, S08

Whitespace "Explained"

Statement	Meaning
[Space][Space][Space] [Tab][LF]	Push 1 onto stack
[LF][Space][Space][Space] [Tab][Space][Space][Space] [Space][Tab][Tab][LF]	Set a label at this point
[Space][LF][Space]	Duplicate the top stack item
[Tab][LF][Space][Tab]	Output the current value
...	...

5
15-213, S08

INTERCAL

Features of INTERCAL

- Designed late one night in 1972 by two Princeton students
- Deliberately obfuscated language

Variables

- 16-bit integers, .1 through .65535
- 32-bit integers, :1 through :65535

Operators

- Binary: "mingle", "select"
- Unary: AND, OR, XOR
 - How are those unary???
 - Simple: AND and's together adjacent bits in a word
- Simplest way to put 65536 in a 32-bit variable?
 - DO :1 <- #0#256

6
15-213, S08

The language “M”

Features of M

- Also designed in the 1970's
- More widely used than Whitespace, INTERCAL

Variables

- 32-bit integer variables: A, B, C, D, DI, F, S, SI
- One array, M[]
 - Valid subscripts range from near zero to a large number
 - But most subscripts in that range will crash your program!

Statements

- Lots of arithmetic and logical operations
- Input and output use a special statement called OUCH!

7

15-213, S'08

A Program in M

C Code

```
int sum(int x, int y)
{
    int t = x+y;
    return t;
}
```

M

```
sum:
    A = M[S+4]
    A += M[S+8]
    DONE
```

8

15-213, S'08

A Program in M

C Code

```
int sum(int x, int y)
{
    int t = x+y;
    return t;
}
```

M

```
sum:
    A = M[S+4]
    A += M[S+8]
    DONE
```

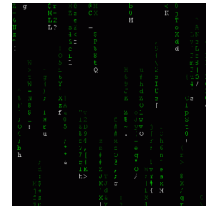
Had enough of M?

- Too bad! We'll study it for much of the semester!
- Why???

9

15-213, S'08

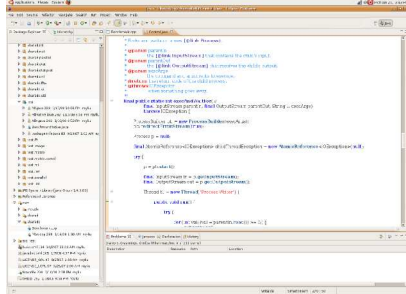
M is “The Language of the Machines”



10

15-213, S'08

Everything Else is Illusion



11

15-213, S'08

IA32 Processors

Totally Dominate Computer Market

Evolutionary Design

- Starting in 1978 with 8086
- Added more features as time goes on
- Still support old features, although obsolete

Complex Instruction Set Computer (CISC)

- Many different instructions with many different formats
 - But, only small subset encountered with Linux programs
- Hard to match performance of Reduced Instruction Set Computers (RISC)
- But, Intel has done just that!

12

15-213, S'08

x86 Evolution: Programmer's View (Abbreviated)

Name	Date	Transistors
8086	1978	29K
16-bit processor. Basis for IBM PC & DOS - Limited to 1MB address space. DOS only gives you 640K		
386	1985	275K
- Extended to 32 bits. Added "flat addressing" - Capable of running Unix - Referred to as "IA32" 32-bit Linux/gcc uses no instructions introduced in later models		

13

15-213, S'08

x86 Evolution: Programmer's View

Machine Evolution

486	1989	1.9M
Pentium	1993	3.1M
Pentium/MMX	1997	4.5M
PentiumPro	1995	6.5M
Pentium III	1999	8.2M
Pentium 4	2001	42M

Added Features

- Instructions to support multimedia operations
 - Parallel operations on 1, 2, and 4-byte data, both integer & FP
- Instructions to enable more efficient conditional operations

Linux/GCC Evolution

- None!

14

15-213, S'08

New Species: IA64

Name	Date	Transistors
Itanium	2001	10M
Extends to IA64, a 64-bit architecture Radically new instruction set designed for high performance Can run existing IA32 programs On-board "x86 engine" Joint project with Hewlett-Packard		
Itanium 2	2002	221M
Big performance boost		
Itanium 2 Dual-Core	2006	1.7B
Itanium has not taken off in marketplace Lack of backward compatibility		

15

15-213, S'08

X86 Evolution: Clones

Advanced Micro Devices (AMD)

- Historically
 - AMD has followed just behind Intel
 - A little bit slower, a lot cheaper
- Recently
 - Recruited top circuit designers from Digital Equipment Corp. and other downward trending companies
 - Exploited fact that Intel distracted by IA64
 - Now are close competitors to Intel
- Developed x86-64, its own extension to 64 bits
 - Started eating into Intel's high-end server market

16

15-213, S'08

Intel's 64-Bit Dilemma

Intel Attempted Radical Shift from IA32 to IA64

- Totally different architecture
- Executes IA32 code only as legacy
- Performance disappointing

AMD Stepped in with Evolutionary Solution

- x86-64 (now called "AMD64")

Intel Felt Obligated to Focus on IA64

- Hard to admit mistake or that AMD is better

2004: Intel Announces EM64T extension to IA32

- Extended Memory 64-bit Technology
- Almost identical to x86-64!
- Our Saltwater fish machines

17

15-213, S'08

Our Coverage

IA32

- The traditional x86

x86-64

- The emerging standard

Presentation

- Book has IA32
- Handout has x86-64
- Lecture will cover both

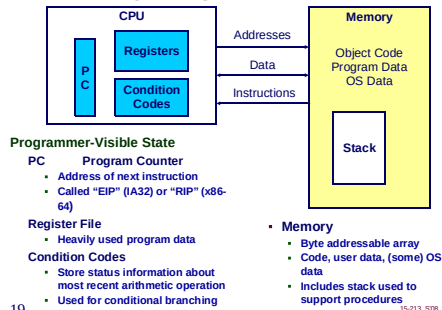
Labs

- Lab #2 x86-64
- Lab #3 IA32

18

15-213, S'08

Assembly Programmer's View

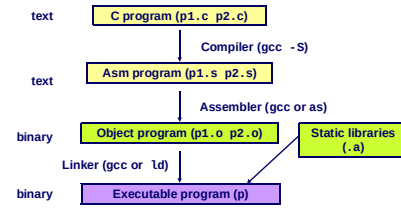


19

15-213, S08

Turning C into Object Code

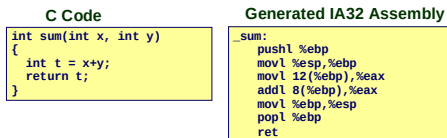
- Code in files `p1.c p2.c`
- Compile with command: `gcc -o p1.c p2.c -o p`
 - Use optimizations (`-O`)
 - Put resulting binary in file `p`



20

15-213, S08

Compiling Into Assembly



Obtain with command
`gcc -O -S code.c`
Produces file `code.s`

21

15-213, S08

Assembly Characteristics

Minimal Data Types

- "Integer" data of 1, 2, or 4 bytes
 - Data values
 - Addresses (untyped pointers)
- Floating point data of 4, 8, or 10 bytes
- No aggregate types such as arrays or structures
 - Just contiguously allocated bytes in memory

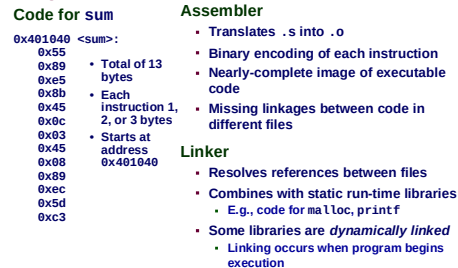
Primitive Operations

- Perform arithmetic function on register or memory data
- Transfer data between memory and register
 - Load data from memory into register
 - Store register data into memory
- Transfer control
 - Unconditional jumps to/from procedures
 - Conditional branches

22

15-213, S08

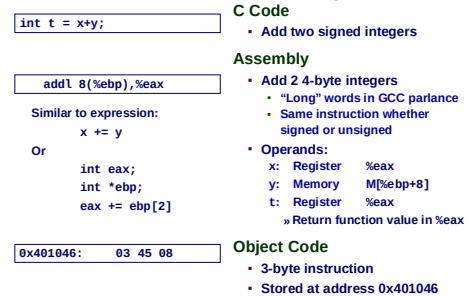
Object Code



23

15-213, S08

Machine Instruction Example



24

15-213, S08

Disassembling Object Code

Disassembled			
00401040	<sum>:		
0:	55	push	%ebp
1:	89 e5	mov	%esp,%ebp
3:	8b 45 0c	mov	0xc(%ebp),%eax
6:	03 45 08	add	0x8(%ebp),%eax
9:	89 ec	mov	%ebp,%esp
b:	5d	pop	%ebp
c:	c3	ret	
d:	8d 76 00	lea	0x0(%esi),%esi

Disassembler

- objdump -d p
- Useful tool for examining object code
- Analyzes bit pattern of series of instructions
- Produces approximate rendition of assembly code
- Can be run on either a .out (complete executable) or .o file

25

15-213, S08

Alternate Disassembly

Disassembled			
0x401040:	0x401040 <sum>:	push	%ebp
0x55	0x401041 <sum+1>:	mov	%esp,%ebp
0x89	0x401043 <sum+3>:	mov	0xc(%ebp),%eax
0xe5	0x401046 <sum+6>:	add	0x8(%ebp),%eax
0x8b	0x401049 <sum+9>:	mov	%ebp,%esp
0x45	0x40104b <sum+11>:	pop	%ebp
0x0c	0x40104c <sum+12>:	ret	
0x03	0x40104d <sum+13>:	lea	0x0(%esi),%esi
0x45			
0x08			
0x89			
0xec			
0x5d			
0xc3			

Within gdb Debugger

- gdb p
- disassemble sum
- Disassemble procedure
- x/13b sum
- Examine the 13 bytes starting at sum

26

15-213, S08

What Can be Disassembled?

```
% objdump -d WINWORD.EXE
WINWORD.EXE: file format pei-i386
No symbols in "WINWORD.EXE".
Disassembly of section .text:
30001000 <.text>:
30001000: 55          push    %ebp
30001001: 8b ec      mov     %esp,%ebp
30001003: 6a ff      push    $0xffffffff
30001005: 68 90 10 00 30 push    $0x30001090
3000100a: 68 91 dc 4c 30 push    $0x304cdc91
```

- Anything that can be interpreted as executable code
- Disassembler examines bytes and reconstructs assembly source

27

15-213, S08

Moving Data: IA32

Moving Data

- movl Source, Dest;
- Move 4-byte ("long") word
- Lots of these in typical code

Operand Types

- Immediate: Constant integer data
 - Like C constant, but prefixed with 'S'
 - E.g., \$0x400, \$-533
 - Encoded with 1, 2, or 4 bytes
- Register: One of 8 integer registers
 - But %esp and %ebp reserved for special use
 - Others have special uses for particular instructions
- Memory: 4 consecutive bytes of memory
 - Various "address modes"

%eax
%edx
%ecx
%ebx
%esi
%edi
%esp
%ebp

28

15-213, S08

movl Operand Combinations

	Source	Dest	Src, Dest	C Analog
movl	Imm	Reg	movl \$0x4,%eax	temp = 0x4;
		Mem	movl \$-147, (%eax)	*p = -147;
	Reg	Reg	movl %eax,%edx	temp2 = temp1;
		Mem	movl %eax, (%edx)	*p = temp;
	Mem	Reg	movl (%eax),%edx	temp = *p;

Cannot do memory-memory transfer with a single instruction

29

15-213, S08

So Many Addressing Modes?

Consider C code

```
struct s {
    double d; // Occupies bytes 0...7
    int i; // Occupies bytes 8...15
    int j; // Occupies bytes 16...23
};

int get_i(struct s *sarray, int which)
{
    return sarray[which].i;
}
```

Where is "sarray[which].i"?

- i starts at byte 8 of a struct...
- ...which is located at (which*16) from the base of sarray
- ...which somebody knows the "base address" of...
- So our value is at M[8 + (base + (which*16))]
- Parts: constant 8, variable which, variable/constant base

30

15-213, S08

Simple Addressing Modes

Normal (R) Mem[Reg[R]]

- Register R specifies memory address

```
movl (%ecx),%eax
```

Displacement D(R) Mem[Reg[R]+D]

- Register R specifies start of memory region
- Constant displacement D specifies offset

```
movl 8(%ebp),%edx
```

31

15-213, S08

Simple Addressing Modes

Normal (R) Mem[Reg[R]]

- Register R specifies memory address

```
movl (%ecx),%eax
```

Displacement D(R) Mem[Reg[R]+D]

- Register R specifies start of memory region
- Constant displacement D specifies offset

```
movl 8(%ebp),%edx
```

32

15-213, S08

Using Simple Addressing Modes

```
void swap(int *xp, int *yp)
{
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    pushl %ebp
    movl %esp,%ebp
    pushl %ebx
    movl 12(%ebp),%ecx
    movl 8(%ebp),%edx
    movl (%ecx),%eax
    movl (%edx),%ebx
    movl %eax,(%edx)
    movl %ebx,(%ecx)
    movl -4(%ebp),%ebx
    movl %ebp,%esp
    popl %ebp
    ret
```

33

15-213, S08

Using Simple Addressing Modes

```
void swap(int *xp, int *yp)
{
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    pushl %ebp
    movl %esp,%ebp
    pushl %ebx
    movl 12(%ebp),%ecx
    movl 8(%ebp),%edx
    movl (%ecx),%eax
    movl (%edx),%ebx
    movl %eax,(%edx)
    movl %ebx,(%ecx)
    movl -4(%ebp),%ebx
    movl %ebp,%esp
    popl %ebp
    ret
```

34

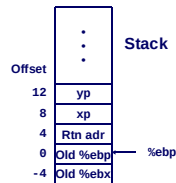
15-213, S08

Understanding Swap

```
void swap(int *xp, int *yp)
{
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

Register	Variable
%ecx	yp
%edx	xp
%eax	t1
%ebx	t0

```
movl 12(%ebp),%ecx # ecx = yp
movl 8(%ebp),%edx # edx = xp
movl (%ecx),%eax # eax = *yp (t1)
movl (%edx),%ebx # ebx = *xp (t0)
movl %eax,(%edx) # *xp = eax
movl %ebx,(%ecx) # *yp = ebx
```

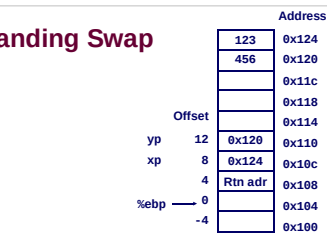


35

15-213, S08

Understanding Swap

%eax	
%edx	
%ecx	
%ebx	
%esi	
%edi	
%esp	
%ebp	0x104

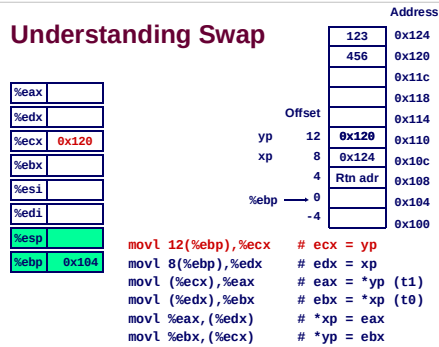


```
movl 12(%ebp),%ecx # ecx = yp
movl 8(%ebp),%edx # edx = xp
movl (%ecx),%eax # eax = *yp (t1)
movl (%edx),%ebx # ebx = *xp (t0)
movl %eax,(%edx) # *xp = eax
movl %ebx,(%ecx) # *yp = ebx
```

36

15-213, S08

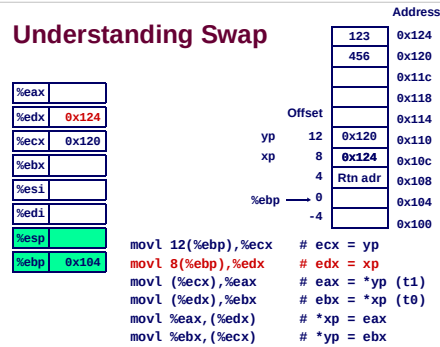
Understanding Swap



37

15-213, 508

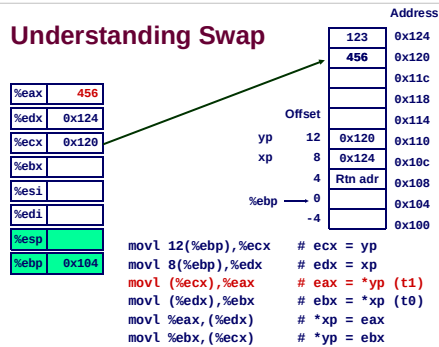
Understanding Swap



38

15-213, 508

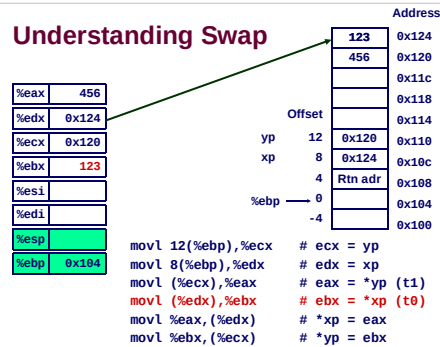
Understanding Swap



39

15-213, 508

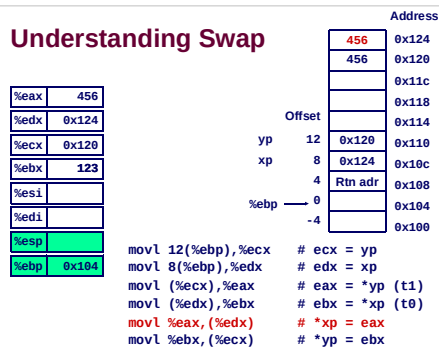
Understanding Swap



40

15-213, 508

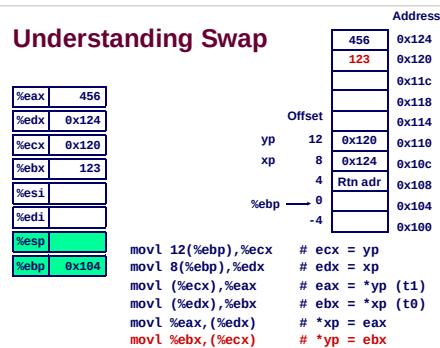
Understanding Swap



41

15-213, 508

Understanding Swap



42

15-213, 508

Indexed Addressing Modes

Most General Form

$D(Rb, Ri, S) \quad Mem[Reg[Rb] + S * Reg[Ri] + D]$

- D: Constant "displacement" 1, 2, or 4 bytes
- Rb: Base register: Any of 8 integer registers
- Ri: Index register: Any, except for %esp
 - Unlikely you'd use %ebp, either
- S: Scale: 1, 2, 4, or 8

Special Cases

$(Rb, Ri) \quad Mem[Reg[Rb] + Reg[Ri]]$

$D(Rb, Ri) \quad Mem[Reg[Rb] + Reg[Ri] + D]$

$(Rb, Ri, S) \quad Mem[Reg[Rb] + S * Reg[Ri]]$

43

15-213, §98

Address Computation Examples

%edx	0xf000
%ecx	0x100

Expression	Computation	Address
0x8(%edx)	0xf000 + 0x8	0xf008
(%edx,%ecx)	0xf000 + 0x100	0xf100
(%edx,%ecx,4)	0xf000 + 4*0x100	0xf400
0x80(,%edx,2)	2*0xf000 + 0x80	0x1e080

44

15-213, §98

Address Computation Instruction

leal Src, Dest

- Src is address mode expression
- Set Dest to address denoted by expression

Uses

- Computing addresses without a memory reference
 - E.g., translation of $p = \&x[i];$
- Computing arithmetic expressions of the form $x + k * y$
 - $k = 1, 2, 4, \text{ or } 8.$

45

15-213, §98

Some Arithmetic Operations

Format Computation

Two-operand Instructions

addl Src, Dest	Dest = Dest + Src
subl Src, Dest	Dest = Dest - Src
imull Src, Dest	Dest = Dest * Src
sall Src, Dest	Dest = Dest << Src Also called shll
sarl Src, Dest	Dest = Dest >> Src Arithmetic
shrl Src, Dest	Dest = Dest >> Src Logical
xorl Src, Dest	Dest = Dest ^ Src
andl Src, Dest	Dest = Dest & Src
orl Src, Dest	Dest = Dest Src

46

15-213, §98

Some Arithmetic Operations

Format Computation

One-operand Instructions

incl Dest	Dest = Dest + 1
decl Dest	Dest = Dest - 1
negl Dest	Dest = - Dest
notl Dest	Dest = ~ Dest

47

15-213, §98

Using leal for Arithmetic Expressions

```

int arith
{
    (int x, int y, int z)
    {
        int t1 = x+y;
        int t2 = z+t1;
        int t3 = x+4;
        int t4 = y * 48;
        int t5 = t3 + t4;
        int rval = t2 * t5;
        return rval;
    }
}
    
```

```

arith:
    pushl %ebp
    movl %esp,%ebp
    movl 8(%ebp),%eax
    movl 12(%ebp),%edx
    leal (%edx,%eax),%ecx
    leal (%edx,%edx,2),%edx
    sall $4,%edx
    addl 16(%ebp),%ecx
    leal 4(%edx,%eax),%eax
    imull %ecx,%eax
    movl %ebp,%esp
    popl %ebp
    ret
    
```

Set Up

Body

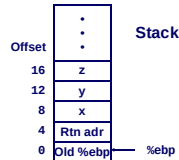
Finish

48

15-213, §98

Understanding arith

```
int arith
(int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```



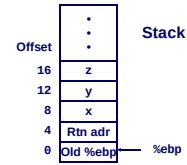
```
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx   # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```

49

15-213, 508

Understanding arith

```
int arith
(int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```



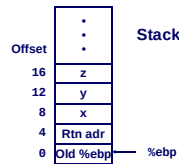
```
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx   # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```

50

15-213, 508

Understanding arith

```
int arith
(int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```



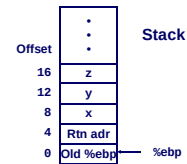
```
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx   # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```

51

15-213, 508

Understanding arith

```
int arith
(int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```



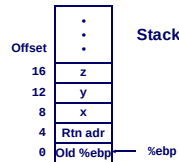
```
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx   # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```

52

15-213, 508

Understanding arith

```
int arith
(int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```



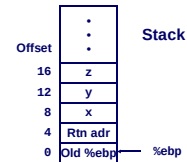
```
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx   # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```

53

15-213, 508

Understanding arith

```
int arith
(int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```



```
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx   # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```

54

15-213, 508

Another Example

```
int logical(int x, int y)
{
    int t1 = x^y;
    int t2 = t1 >> 17;
    int mask = (1<<13) - 7;
    int rval = t2 & mask;
    return rval;
}
```

logical:

```

pushl %ebp          } Set Up
movl %esp,%ebp

movl 8(%ebp),%eax    }
xorl 12(%ebp),%eax   }
sarl $17,%eax        } Body
andl $8185,%eax      }

movl %ebp,%esp       }
popl %ebp            } Finish
ret
```

```

movl 8(%ebp),%eax    eax = x
xorl 12(%ebp),%eax   eax = x^y
sarl $17,%eax        eax = t1>>17
andl $8185,%eax      eax = t2 & 8185
```

55

15-213, §08

Another Example

```
int logical(int x, int y)
{
    int t1 = x^y;
    int t2 = t1 >> 17;
    int mask = (1<<13) - 7;
    int rval = t2 & mask;
    return rval;
}
```

logical:

```

pushl %ebp          } Set Up
movl %esp,%ebp

movl 8(%ebp),%eax    }
xorl 12(%ebp),%eax   }
sarl $17,%eax        } Body
andl $8185,%eax      }

movl %ebp,%esp       }
popl %ebp            } Finish
ret
```

```

movl 8(%ebp),%eax    eax = x
xorl 12(%ebp),%eax   eax = x^y (t1)
sarl $17,%eax        eax = t1>>17 (t2)
andl $8185,%eax      eax = t2 & 8185
```

56

15-213, §08

Another Example

```
int logical(int x, int y)
{
    int t1 = x^y;
    int t2 = t1 >> 17;
    int mask = (1<<13) - 7;
    int rval = t2 & mask;
    return rval;
}
```

logical:

```

pushl %ebp          } Set Up
movl %esp,%ebp

movl 8(%ebp),%eax    }
xorl 12(%ebp),%eax   }
sarl $17,%eax        } Body
andl $8185,%eax      }

movl %ebp,%esp       }
popl %ebp            } Finish
ret
```

```

movl 8(%ebp),%eax    eax = x
xorl 12(%ebp),%eax   eax = x^y (t1)
sarl $17,%eax        eax = t1>>17 (t2)
andl $8185,%eax      eax = t2 & 8185
```

57

15-213, §08

Another Example

```
int logical(int x, int y)
{
    int t1 = x^y;
    int t2 = t1 >> 17;
    int mask = (1<<13) - 7;
    int rval = t2 & mask;
    return rval;
}
```

logical:

```

pushl %ebp          } Set Up
movl %esp,%ebp

movl 8(%ebp),%eax    }
xorl 12(%ebp),%eax   }
sarl $17,%eax        } Body
andl $8185,%eax      }

movl %ebp,%esp       }
popl %ebp            } Finish
ret
```

$2^{13} = 8192, 2^{13} - 7 = 8185$

```

movl 8(%ebp),%eax    eax = x
xorl 12(%ebp),%eax   eax = x^y (t1)
sarl $17,%eax        eax = t1>>17 (t2)
andl $8185,%eax      eax = t2 & 8185 (rval)
```

58

15-213, §08

Data Representations: IA32 + x86-64

Sizes of C Objects (in Bytes)

C Data Type	Typical 32-bit	Intel IA32	x86-64
unsigned	4	4	4
int	4	4	4
long int	4	4	8
char	1	1	1
short	2	2	2
float	4	4	4
double	8	8	8
long double	8	10/12	16
char *	4	4	8

» Or any other pointer

59

15-213, §08

x86-64 General Purpose Registers

%rax	%eax	%r8	%r8d
%rdx	%edx	%r9	%r9d
%rcx	%ecx	%r10	%r10d
%rbx	%ebx	%r11	%r11d
%rsi	%esi	%r12	%r12d
%rdi	%edi	%r13	%r13d
%rsp	%esp	%r14	%r14d
%rbp	%ebp	%r15	%r15d

• Extend existing registers. Add 8 new ones.

60* Make %ebp/%rbp general purpose

15-213, §08

Swap in 32-bit Mode

```
void swap(int *xp, int *yp)
{
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    pushl %ebp
    movl %esp,%ebp
    pushl %ebx
    movl 12(%ebp),%ecx
    movl 8(%ebp),%edx
    movl (%ecx),%eax
    movl (%edx),%ebx
    movl %eax, (%edx)
    movl %ebx, (%ecx)
    movl -4(%ebp),%ebx
    movl %ebp,%esp
    popl %ebp
    ret
```

Set Up

Body

Finish

61

15-213, S08

Swap in 64-bit Mode

```
void swap(int *xp, int *yp)
{
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    movl (%rdi), %edx
    movl (%rsi), %eax
    movl %eax, (%rdi)
    movl %edx, (%rsi)
    ret
```

- Operands passed in registers
 - First (xp) in %rdi, second (yp) in %rsi
 - 64-bit pointers
- No stack operations required
- 32-bit data
 - Data held in registers %eax and %edx
 - movl operation

62

15-213, S08

Swap Long Ints in 64-bit Mode

```
void swap_l
(long int *xp, long int *yp)
{
    long int t0 = *xp;
    long int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap_l:
    movq (%rdi), %rdx
    movq (%rsi), %rax
    movq %rax, (%rdi)
    movq %rdx, (%rsi)
    ret
```

- 64-bit data
 - Data held in registers %rax and %rdx
 - movq operation
 - "q" stands for quad-word

63

15-213, S08

Summary

Machine Level Programming

- Assembly code is textual form of binary object code
- Low-level representation of program
 - Explicit manipulation of registers
 - Simple and explicit instructions
 - Minimal concept of data types
 - Many C control constructs must be implemented with multiple instructions

Formats

- IA32: Historical x86 format
- x86-64: Big evolutionary step

64

15-213, S08

Credits

Languages

- <http://compsoc.dur.ac.uk/whitespace/>
- <http://catb.org/~esr/intercal/>

Screen shots

- <http://mgccl.com/2007/03/30/simple-version-matrix-like-animated-dropping-character-effect-in-php>
- Eclipse shot courtesy of Roy Liu, <http://hubris.ucsd.edu>

65

15-213, S08