15-213
“The course that gives CMU its Zip!”

Machine-Level Programming I: Introduction
Sept. 9, 2003

Topics

- Assembly Programmer’s Execution Model
- Accessing Information
  - Registers
  - Memory
- Arithmetic operations

class05.ppt
IA32 Processors

Totally Dominate Computer Market

Evolutionary Design

- Starting in 1978 with 8086
- Added more features as time goes on
- Still support old features, although obsolete

Complex Instruction Set Computer (CISC)

- Many different instructions with many different formats
  - But, only small subset encountered with Linux programs
- Hard to match performance of Reduced Instruction Set Computers (RISC)
- But, Intel has done just that!
# X86 Evolution: Programmer’s View

<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>8086</td>
<td>1978</td>
<td>29K</td>
</tr>
<tr>
<td>80286</td>
<td>1982</td>
<td>134K</td>
</tr>
<tr>
<td>386</td>
<td>1985</td>
<td>275K</td>
</tr>
</tbody>
</table>

- 16-bit processor. Basis for IBM PC & DOS
- Limited to 1MB address space. DOS only gives you 640K

- Added elaborate, but not very useful, addressing scheme
- Basis for IBM PC-AT and Windows

- Extended to 32 bits. Added “flat addressing”
- Capable of running Unix
- Linux/gcc uses no instructions introduced in later models
## X86 Evolution: Programmer’s View

<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>486</td>
<td>1989</td>
<td>1.9M</td>
</tr>
<tr>
<td>Pentium</td>
<td>1993</td>
<td>3.1M</td>
</tr>
<tr>
<td>Pentium/MMX</td>
<td>1997</td>
<td>4.5M</td>
</tr>
<tr>
<td><strong>PentiumPro</strong></td>
<td>1995</td>
<td>6.5M</td>
</tr>
</tbody>
</table>

- Added special collection of instructions for operating on 64-bit vectors of 1, 2, or 4 byte integer data
- Added conditional move instructions
- Big change in underlying microarchitecture
# X86 Evolution: Programmer’s View

<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pentium III</td>
<td>1999</td>
<td>8.2M</td>
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<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pentium 4</td>
<td>2001</td>
<td>42M</td>
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</tbody>
</table>

- Added “streaming SIMD” instructions for operating on 128-bit vectors of 1, 2, or 4 byte integer or floating point data
- Our fish machines

- Added 8-byte formats and 144 new instructions for streaming SIMD mode
X86 Evolution: Clones

Advanced Micro Devices (AMD)

- Historically
  - AMD has followed just behind Intel
  - A little bit slower, a lot cheaper

- Recently
  - Recruited top circuit designers from Digital Equipment Corp.
  - Exploited fact that Intel distracted by IA64
  - Now are close competitors to Intel

- Developing own extension to 64 bits
X86 Evolution: Clones

Transmeta

- Recent start-up
  - Employer of Linus Torvalds
- Radically different approach to implementation
  - Translates x86 code into “Very Long Instruction Word” (VLIW) code
  - High degree of parallelism
- Shooting for low-power market
## New Species: IA64

<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium</td>
<td>2001</td>
<td>10M</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Extends to IA64, a 64-bit architecture</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Radically new instruction set designed for high performance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Will be able to run existing IA32 programs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- On-board “x86 engine”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Joint project with Hewlett-Packard</td>
</tr>
<tr>
<td>Itanium 2</td>
<td>2002</td>
<td>221M</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Big performance boost</td>
</tr>
</tbody>
</table>
Assembly Programmer’s View

Programmer-Visible State

- **EIP** Program Counter
  - Address of next instruction

- **Register File**
  - Heavily used program data

- **Condition Codes**
  - Store status information about most recent arithmetic operation
  - Used for conditional branching

**Memory**

- Byte addressable array
- Code, user data, (some) OS data
- Includes stack used to support procedures

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15-213, F’03
Turning C into Object Code

- Code in files \texttt{p1.c p2.c}
- Compile with command: \texttt{gcc -O p1.c p2.c -o p}
  - Use optimizations (-O)
  - Put resulting binary in file \texttt{p}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{diagram.png}
\end{figure}
Compiling Into Assembly

C Code

```c
int sum(int x, int y)
{
    int t = x + y;
    return t;
}
```

Generated Assembly

```assembly
_sum:
pushl %ebp
movl %esp, %ebp
movl 12(%ebp), %eax
addl 8(%ebp), %eax
movl %ebp, %esp
popl %ebp
ret
```

Obtain with command

```
gcc -O -S code.c
```

Produces file `code.s`
Assembly Characteristics

Minimal Data Types

- “Integer” data of 1, 2, or 4 bytes
  - Data values
  - Addresses (untyped pointers)
- Floating point data of 4, 8, or 10 bytes
- No aggregate types such as arrays or structures
  - Just contiguously allocated bytes in memory

Primitive Operations

- Perform arithmetic function on register or memory data
- Transfer data between memory and register
  - Load data from memory into register
  - Store register data into memory
- Transfer control
  - Unconditional jumps to/from procedures
  - Conditional branches
Object Code

Code for sum

0x401040 <sum>:

0x55
0x89
0xe5
0x8b
0x45
0x0c
0x03
0x45
0x08
0x89
0xec
0x5d
0xc3

- Total of 13 bytes
- Each instruction 1, 2, or 3 bytes
- Starts at address 0x401040

Assembler

- Translates .s into .o
- Binary encoding of each instruction
- Nearly-complete image of executable code
- Missing linkages between code in different files

Linker

- Resolves references between files
- Combines with static run-time libraries
  - E.g., code for malloc, printf
- Some libraries are dynamically linked
  - Linking occurs when program begins execution
Machine Instruction Example

C Code

```c
int t = x+y;
```

- Add two signed integers

Assembly

- Add 2 4-byte integers
  - “Long” words in GCC parlance
  - Same instruction whether signed or unsigned

- Operands:
  - \( x \): Register \%eax
  - \( y \): Memory \( M[\%ebp+8] \)
  - \( t \): Register \%eax
    » Return function value in \%eax

Object Code

- 3-byte instruction
- Stored at address 0x401046
Disassembling Object Code

Disassembled

<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>00401040</td>
<td><code>&lt;_sum&gt;</code>:</td>
<td></td>
</tr>
<tr>
<td>0:</td>
<td>55 <code>push %ebp</code></td>
<td></td>
</tr>
<tr>
<td>1:</td>
<td>89 e5 <code>mov %esp,%ebp</code></td>
<td></td>
</tr>
<tr>
<td>3:</td>
<td>8b 45 0c <code>mov 0xc(%ebp),%eax</code></td>
<td></td>
</tr>
<tr>
<td>6:</td>
<td>03 45 08 <code>add 0x8(%ebp),%eax</code></td>
<td></td>
</tr>
<tr>
<td>9:</td>
<td>89 ec <code>mov %ebp,%esp</code></td>
<td></td>
</tr>
<tr>
<td>b:</td>
<td>5d <code>pop %ebp</code></td>
<td></td>
</tr>
<tr>
<td>c:</td>
<td>c3 <code>ret</code></td>
<td></td>
</tr>
<tr>
<td>d:</td>
<td>8d 76 00 <code>lea 0x0(%esi),%esi</code></td>
<td></td>
</tr>
</tbody>
</table>

Disassembler

objdump -d p

- Useful tool for examining object code
- Analyzes bit pattern of series of instructions
- Produces approximate rendition of assembly code
- Can be run on either a .out (complete executable) or .o file
Alternate Disassembly

Disassembled

Object

Disassembled

Within gdb Debugger

gdb p
disable sum

Disassemble procedure

x/13b sum

Examine the 13 bytes starting at sum
What Can be Disassembled?

% objdump -d WINWORD.EXE

WINWORD.EXE: file format pei-i386

No symbols in "WINWORD.EXE".
Disassembly of section .text:

30001000 <.text>:
30001000: 55              push %ebp
30001001: 8b ec           mov %esp,%ebp
30001003: 6a ff           push $0xffffffff
30001005: 68 90 10 00 30 push $0x30001090
3000100a: 68 91 dc 4c 30 push $0x304cdc91

- Anything that can be interpreted as executable code
- Disassembler examines bytes and reconstructs assembly source
Moving Data

movl Source, Dest:
- Move 4-byte (“long”) word
- Lots of these in typical code

Operand Types
- Immediate: Constant integer data
  - Like C constant, but prefixed with ‘$’
  - E.g., $0x400, $-533
  - Encoded with 1, 2, or 4 bytes
- Register: One of 8 integer registers
  - But %esp and %ebp reserved for special use
  - Others have special uses for particular instructions
- Memory: 4 consecutive bytes of memory
  - Various “address modes”
**movl** **Operand Combinations**

<table>
<thead>
<tr>
<th>Source</th>
<th>Destination</th>
<th>C Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Imm</strong></td>
<td><strong>Reg</strong></td>
<td><strong>movl</strong> $0x4, %eax</td>
</tr>
<tr>
<td><strong>Imm</strong></td>
<td><strong>Mem</strong></td>
<td><strong>movl</strong> $-147, (%eax)</td>
</tr>
<tr>
<td><strong>Reg</strong></td>
<td><strong>Reg</strong></td>
<td><strong>movl</strong> %eax, %edx</td>
</tr>
<tr>
<td><strong>Reg</strong></td>
<td><strong>Mem</strong></td>
<td><strong>movl</strong> %eax, (%edx)</td>
</tr>
<tr>
<td><strong>Mem</strong></td>
<td><strong>Reg</strong></td>
<td><strong>movl</strong> (%eax), %edx</td>
</tr>
</tbody>
</table>

- Cannot do memory-memory transfers with single instruction
Simple Addressing Modes

Normal (R) Mem[Reg[R]]
- Register R specifies memory address
  movl (%ecx), %eax

Displacement D(R) Mem[Reg[R]+D]
- Register R specifies start of memory region
- Constant displacement D specifies offset
  movl 8(%ebp), %edx
Using Simple Addressing Modes

```c
void swap(int *xp, int *yp)
{
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    pushl %ebp
    movl %esp,%ebp
    pushl %ebx

    movl 12(%ebp),%ecx
    movl 8(%ebp),%edx
    movl (%ecx),%eax
    movl (%edx),%ebx
    movl %eax,(%edx)
    movl %ebx,(%ecx)

    movl -4(%ebp),%ebx
    movl %ebp,%esp
    popl %ebp
    ret
```
void swap(int *xp, int *yp) {
    int t0 = *xp;
    int t1 = *yp;
    *xp = t1;
    *yp = t0;
}

movl 12(%ebp),%ecx  # ecx = yp
movl 8(%ebp),%edx  # edx = xp
movl (%ecx),%eax  # eax = *yp (t1)
movl (%edx),%ebx  # ebx = *xp (t0)
movl %eax,(%edx)  # *xp = eax
movl %ebx,(%ecx)  # *yp = ebx
Understanding Swap

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
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<tbody>
<tr>
<td>%eax</td>
<td>0x120</td>
</tr>
<tr>
<td>%edx</td>
<td>0x124</td>
</tr>
<tr>
<td>%ecx</td>
<td>0x128</td>
</tr>
<tr>
<td>%ebx</td>
<td>0x130</td>
</tr>
<tr>
<td>%esi</td>
<td>0x134</td>
</tr>
<tr>
<td>%edi</td>
<td>0x138</td>
</tr>
<tr>
<td>%esp</td>
<td>0x140</td>
</tr>
<tr>
<td>%ebp</td>
<td>0x144</td>
</tr>
</tbody>
</table>

offsets:

<table>
<thead>
<tr>
<th>Address</th>
<th>Offset</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x100</td>
<td>0</td>
<td>%ebp</td>
</tr>
<tr>
<td>0x104</td>
<td>4</td>
<td>%edi</td>
</tr>
<tr>
<td>0x108</td>
<td>8</td>
<td>%edx</td>
</tr>
<tr>
<td>0x110</td>
<td>12</td>
<td>%ecx</td>
</tr>
<tr>
<td>0x114</td>
<td>16</td>
<td>%esp</td>
</tr>
<tr>
<td>0x118</td>
<td>20</td>
<td>%esi</td>
</tr>
<tr>
<td>0x120</td>
<td>24</td>
<td>%eax</td>
</tr>
<tr>
<td>0x124</td>
<td>28</td>
<td>%ebp</td>
</tr>
<tr>
<td>0x128</td>
<td>32</td>
<td>%ecx</td>
</tr>
</tbody>
</table>

- movl 12(%ebp),%ecx  # ecx = yp
- movl 8(%ebp),%edx  # edx = xp
- movl (%ecx),%eax  # eax = *yp (t1)
- movl (%edx),%ebx  # ebx = *xp (t0)
- movl %eax, (%edx)  # *xp = eax
- movl %ebx, (%ecx)  # *yp = ebx
Understanding Swap

\[
\begin{align*}
\text{movl} \ 12(\%ebp),\%ecx & \quad \# \ ecx = yp \\
\text{movl} \ 8(\%ebp),\%edx & \quad \# \ edx = xp \\
\text{movl} \ (\%ecx),\%eax & \quad \# \ eax = *yp \ (t1) \\
\text{movl} \ (\%edx),\%ebx & \quad \# \ ebx = *xp \ (t0) \\
\text{movl} \ %eax,(\%edx) & \quad \# \ *xp = eax \\
\text{movl} \ %ebx,(\%ecx) & \quad \# \ *yp = ebx
\end{align*}
\]
Understanding Swap

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<tr>
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</tr>
<tr>
<td>%ecx</td>
<td>0x120</td>
</tr>
<tr>
<td>%ebx</td>
<td>0x104</td>
</tr>
<tr>
<td>%esi</td>
<td>0x114</td>
</tr>
<tr>
<td>%edi</td>
<td>0x108</td>
</tr>
<tr>
<td>%esp</td>
<td>0x120</td>
</tr>
<tr>
<td>%ebp</td>
<td>0x104</td>
</tr>
</tbody>
</table>

### Instructions

- `movl 12(%ebp),%ecx`  # ecx = yp
- `movl 8(%ebp),%edx`  # edx = xp
- `movl (%ecx),%eax`  # eax = *yp (t1)
- `movl (%edx),%ebx`  # ebx = *xp (t0)
- `movl %eax,(%edx)`  # *xp = eax
- `movl %ebx,(%ecx)`  # *yp = ebx

### Offsets

<table>
<thead>
<tr>
<th>Offset</th>
<th>Address</th>
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</thead>
<tbody>
<tr>
<td>YP</td>
<td>0x120</td>
</tr>
<tr>
<td>XP</td>
<td>0x124</td>
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<tr>
<td>Rtn adr</td>
<td>0x108</td>
</tr>
<tr>
<td></td>
<td>0x104</td>
</tr>
<tr>
<td></td>
<td>0x100</td>
</tr>
</tbody>
</table>
## Understanding Swap

### Registers and Addresses

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>%eax</td>
<td>456</td>
</tr>
<tr>
<td>%edx</td>
<td>0x124</td>
</tr>
<tr>
<td>%ecx</td>
<td>0x120</td>
</tr>
<tr>
<td>%ebx</td>
<td></td>
</tr>
<tr>
<td>%esi</td>
<td></td>
</tr>
<tr>
<td>%edi</td>
<td></td>
</tr>
<tr>
<td>%esp</td>
<td></td>
</tr>
<tr>
<td>%ebp</td>
<td>0x104</td>
</tr>
</tbody>
</table>

### MOV Instructions

- `movl 12(%ebp),%ecx` # ecx = yp
- `movl 8(%ebp),%edx` # edx = xp
- `movl (%ecx),%eax` # eax = *yp (t1)
- `movl (%edx),%ebx` # ebx = *xp (t0)
- `movl %eax,(%edx)` # *xp = eax
- `movl %ebx,(%ecx)` # *yp = ebx
Understanding Swap

movl 12(%ebp),%ecx  # ecx = yp
movl 8(%ebp),%edx  # edx = xp
movl (%ecx),%eax  # eax = *yp (t1)
movl (%edx),%ebx  # ebx = *xp (t0)
movl %eax,(%edx)  # *xp = eax
movl %ebx,(%ecx)  # *yp = ebx
Understanding Swap

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>%eax</td>
<td>0x124</td>
</tr>
<tr>
<td>%edx</td>
<td>0x110</td>
</tr>
<tr>
<td>%ecx</td>
<td>0x10c</td>
</tr>
<tr>
<td>%ebx</td>
<td>0x108</td>
</tr>
<tr>
<td>%esi</td>
<td></td>
</tr>
<tr>
<td>%edi</td>
<td></td>
</tr>
<tr>
<td>%esp</td>
<td>0x104</td>
</tr>
<tr>
<td>%ebp</td>
<td>0x100</td>
</tr>
</tbody>
</table>

movl 12(%ebp),%ecx  # ecx = yp
movl 8(%ebp),%edx  # edx = xp
movl (%ecx),%eax   # eax = *yp (t1)
movl (%edx),%ebx   # ebx = *xp (t0)
movl %eax,%edx     # *xp = eax
movl %ebx,%ecx     # *yp = ebx

Address

<table>
<thead>
<tr>
<th>Offset</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>0x120</td>
</tr>
<tr>
<td>8</td>
<td>0x124</td>
</tr>
<tr>
<td>4</td>
<td>Rtn adr</td>
</tr>
<tr>
<td>0</td>
<td>0x108</td>
</tr>
<tr>
<td>-4</td>
<td>0x104</td>
</tr>
</tbody>
</table>

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Understanding Swap

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>%eax</td>
<td>456</td>
</tr>
<tr>
<td>%edx</td>
<td>0x124</td>
</tr>
<tr>
<td>%ecx</td>
<td>0x120</td>
</tr>
<tr>
<td>%ebx</td>
<td>123</td>
</tr>
<tr>
<td>%esi</td>
<td></td>
</tr>
<tr>
<td>%edi</td>
<td></td>
</tr>
<tr>
<td>%esp</td>
<td></td>
</tr>
<tr>
<td>%ebp</td>
<td>0x104</td>
</tr>
</tbody>
</table>

```
movl 12(%ebp), %ecx  # ecx = yp
movl 8(%ebp), %edx   # edx = xp
movl (%ecx), %eax    # eax = *yp (t1)
movl (%edx), %ebx    # ebx = *xp (t0)
movl %eax, (%edx)   # *xp = eax
movl %ebx, (%ecx)   # *yp = ebx
```
Indexed Addressing Modes

Most General Form

\[ D(Rb, Ri, S) \quad \text{Mem}[\text{Reg}[Rb] + S*\text{Reg}[Ri] + D] \]

- **D**: Constant “displacement” 1, 2, or 4 bytes
- **Rb**: Base register: Any of 8 integer registers
- **Ri**: Index register: Any, except for %esp
  - Unlikely you’d use %ebp, either
- **S**: Scale: 1, 2, 4, or 8

Special Cases

\[ (Rb, Ri) \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri]] \]
\[ D(Rb, Ri) \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] + D] \]
\[ (Rb, Ri, S) \quad \text{Mem}[\text{Reg}[Rb] + S*\text{Reg}[Ri]] \]
# Address Computation Examples

<table>
<thead>
<tr>
<th>Expression</th>
<th>Computation</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8(%edx)</td>
<td>0xf000 + 0x8</td>
<td>0xf008</td>
</tr>
<tr>
<td>(%edx,%ecx)</td>
<td>0xf000 + 0x100</td>
<td>0xf100</td>
</tr>
<tr>
<td>(%edx,%ecx,4)</td>
<td>0xf000 + 4*0x100</td>
<td>0xf400</td>
</tr>
<tr>
<td>0x80(,%edx,2)</td>
<td>2*0xf000 + 0x80</td>
<td>0x1e080</td>
</tr>
</tbody>
</table>
Address Computation Instruction

`lea `Src,`Dest`

- `Src` is address mode expression
- Set `Dest` to address denoted by expression

Uses

- Computing address without doing memory reference
  - E.g., translation of `p = &x[i];`
- Computing arithmetic expressions of the form `x + k*y`
  - `k = 1, 2, 4,` or `8.`
### Some Arithmetic Operations

<table>
<thead>
<tr>
<th>Format</th>
<th>Computation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Two Operand Instructions</strong></td>
<td></td>
</tr>
<tr>
<td>addl ( Src, Dest )</td>
<td>( Dest = Dest + Src )</td>
</tr>
<tr>
<td>subl ( Src, Dest )</td>
<td>( Dest = Dest - Src )</td>
</tr>
<tr>
<td>imull ( Src, Dest )</td>
<td>( Dest = Dest \times Src )</td>
</tr>
<tr>
<td>sal1 ( Src, Dest )</td>
<td>( Dest = Dest \ll Src ) Also called \texttt{shll}</td>
</tr>
<tr>
<td>sarl ( Src, Dest )</td>
<td>( Dest = Dest \gg Src ) Arithmetic</td>
</tr>
<tr>
<td>shr1 ( Src, Dest )</td>
<td>( Dest = Dest \gg Src ) Logical</td>
</tr>
<tr>
<td>xorl ( Src, Dest )</td>
<td>( Dest = Dest ^{} Src )</td>
</tr>
<tr>
<td>andl ( Src, Dest )</td>
<td>( Dest = Dest &amp; Src )</td>
</tr>
<tr>
<td>orl ( Src, Dest )</td>
<td>( Dest = Dest \mid Src )</td>
</tr>
</tbody>
</table>
# Some Arithmetic Operations

<table>
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<tr>
<td><strong>One Operand Instructions</strong></td>
<td></td>
</tr>
<tr>
<td>incl Dest</td>
<td>Dest = Dest + 1</td>
</tr>
<tr>
<td>decl Dest</td>
<td>Dest = Dest - 1</td>
</tr>
<tr>
<td>negl Dest</td>
<td>Dest = - Dest</td>
</tr>
<tr>
<td>notl Dest</td>
<td>Dest = ~ Dest</td>
</tr>
</tbody>
</table>
Using _lea1 for Arithmetic Expressions_

```c
int arith
    (int x, int y, int z)
{
    int t1 = x+y;
    int t2 = z+t1;
    int t3 = x+4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```

```
arith:
    pushl %ebp
    movl %esp,%ebp
    movl 8(%ebp),%eax
    movl 12(%ebp),%edx
    leal (%edx,%eax),%ecx
    leal (%edx,%edx,2),%edx
    sall $4,%edx
    addl 16(%ebp),%ecx
    leal 4(%edx,%eax),%eax
    imull %ecx,%eax
    movl %ebp,%esp
    popl %ebp
    ret
```
Understanding arith

```c
int arith
    (int x, int y, int z)
{
    int t1 = x + y;
    int t2 = z + t1;
    int t3 = x + 4;
    int t4 = y * 48;
    int t5 = t3 + t4;
    int rval = t2 * t5;
    return rval;
}
```

```assembly
movl 8(%ebp),%eax    # eax = x
movl 12(%ebp),%edx   # edx = y
leal (%edx,%eax),%ecx # ecx = x+y (t1)
leal (%edx,%edx,2),%edx # edx = 3*y
sall $4,%edx         # edx = 48*y (t4)
addl 16(%ebp),%ecx    # ecx = z+t1 (t2)
leal 4(%edx,%eax),%eax # eax = 4+t4+x (t5)
imull %ecx,%eax      # eax = t5*t2 (rval)
```
int arith
  (int x, int y, int z)
{
  int t1 = x+y;
  int t2 = z+t1;
  int t3 = x+4;
  int t4 = y * 48;
  int t5 = t3 + t4;
  int rval = t2 * t5;
  return rval;
}
Another Example

int logical(int x, int y)
{
    int t1 = x^y;
    int t2 = t1 >> 17;
    int mask = (1<<13) - 7;
    int rval = t2 & mask;
    return rval;
}

logical:
    pushl %ebp
    movl %esp,%ebp

    movl 8(%ebp),%eax
    xorl 12(%ebp),%eax
    sarl $17,%eax
    andl $8185,%eax

    movl %ebp,%esp
    popl %ebp
    ret

\[
2^{13} = 8192, \quad 2^{13} - 7 = 8185
\]
**CISC Properties**

**Instruction can reference different operand types**
- Immediate, register, memory

**Arithmetic operations can read/write memory**

**Memory reference can involve complex computation**
- \( Rb + S^*Ri + D \)
- Useful for arithmetic expressions, too

**Instructions can have varying lengths**
- IA32 instructions can range from 1 to 15 bytes
Summary: Abstract Machines

Machine Models

Data

1) char
2) int, float
3) double
4) struct, array
5) pointer

Control

1) loops
2) conditionals
3) switch
4) Proc. call
5) Proc. return

Assembly

1) byte
2) 2-byte word
3) branch/jump
4) 4-byte long word
5) call
6) contiguous byte allocation
5) ret

address of initial byte
Pentium Pro (P6)

History
- Announced in Feb. ‘95
- Basis for Pentium II, Pentium III, and Celeron processors
- Pentium 4 similar idea, but different details

Features
- Dynamically translates instructions to more regular format
  - Very wide, but simple instructions
- Executes operations in parallel
  - Up to 5 at once
- Very deep pipeline
  - 12–18 cycle latency
Pentium Pro Block Diagram
Pentium Pro Operation

Translates instructions dynamically into “Uops”
- 118 bits wide
- Holds operation, two sources, and destination

Executes Uops with “Out of Order” engine
- Uop executed when
  - Operands available
  - Functional unit available
- Execution controlled by “Reservation Stations”
  - Keeps track of data dependencies between uops
  - Allocates resources

Consequences
- Indirect relationship between IA32 code & what actually gets executed
- Tricky to predict / optimize performance at assembly level
## Whose Assembler?

### Intel/Microsoft Format

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>lea</td>
<td>eax, [ecx+ecx*2]</td>
</tr>
<tr>
<td>sub</td>
<td>esp, 8</td>
</tr>
<tr>
<td>cmp</td>
<td>dword ptr [ebp-8], 0</td>
</tr>
<tr>
<td>mov</td>
<td>eax, dword ptr [eax*4+100h]</td>
</tr>
</tbody>
</table>

### GAS/Gnu Format

<table>
<thead>
<tr>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>leal</td>
<td>(%ecx,%ecx,2),%eax</td>
</tr>
<tr>
<td>subl</td>
<td>$8,%esp</td>
</tr>
<tr>
<td>cmpl</td>
<td>$0,-8(%ebp)</td>
</tr>
<tr>
<td>movl</td>
<td>$0x100(,%eax,4),%eax</td>
</tr>
</tbody>
</table>

### Intel/Microsoft Differs from GAS

- **Operands listed in opposite order**
  
  - `mov Dest, Src`  
  - `movl Src, Dest`

- **Constants not preceded by ‘$’, Denote hex with ‘h’ at end**
  
  - `100h`  
  - `$0x100`

- **Operand size indicated by operands rather than operator suffix**
  
  - `sub`  
  - `subl`

- **Addressing format shows effective address computation**
  
  - `[eax*4+100h]`  
  - `$0x100(,%eax,4)`