Carnegie Mellon University
Computer Science Department

THESIS ORAL

YIXIN LUO

Architectural Techniques for Improving NAND Flash Memory Reliability

Friday, February 9, 2018 – 9:00 a.m. – GHC 6501

Raw bit errors are common in NAND flash memory and will increase in the future. These errors reduce flash reliability and limit the lifetime of a flash memory device. This dissertation improves flash reliability with a multitude of low-cost architectural techniques. We show that NAND flash memory reliability can be improved at low cost and with low performance overhead by deploying various architectural techniques that are aware of higher-level application behavior and underlying flash device characteristics.

This dissertation analyzes flash error characteristics and workload behavior through rigorous experimental characterization and designs new flash controller algorithms that use the insights gained from our analysis to improve flash reliability at low cost. We investigate four novel directions. (1) We propose a new technique called WARM that improves flash lifetime by 12.9 times by managing flash retention differently for write-hot data and write-cold data. (2) We propose a new framework that learns an online flash channel model for each chip and enables four new flash controller algorithms to improve flash write endurance by up to 69.9%. (3) We identify three new error characteristics in 3D NAND flash memory through comprehensive experimental characterization of real 3D NAND chips, and propose four new techniques that mitigate these new errors and improve 3D NAND raw bit error rate by up to 66.9%. (4) We propose a new technique called HeatWatch that improves 3D NAND lifetime by 3.85 times by utilizing the self-healing effect to mitigate retention errors in 3D NAND.

Thesis Committee:
Onur Mutlu, Chair
Phillip B. Gibbons
James C. Hoe
Erich F. Haratsch, Seagate
Yu Cai, SK Hynix