We start by quickly reviewing 50 years of computer architecture to show there is now widespread agreement on instruction set architecture (ISA). Unlike most other fields, despite this harmony there is no open alternative to proprietary offerings from ARM and Intel. Thus, we propose RISC-V (“RISC Five”), which targets Systems on a Chip (SoC). It has:

- A small base of <50 classic RISC instructions that run a full open-source software stack.
- Opcodes reserved for tailoring an SoC to applications.
- Standard instruction extensions optionally included in an SoC.
- Incorporated, as an open ISA, community suggestions before extensions are finalized.
- A foundation to evolve the RISC-V slowly based solely on technical reasons voted on by members vs. by companies that inflate ISAs rapidly for business as well as technical reasons; ARM and Intel average about 2 new instructions per month.
- No restrictions: there is no cost, no paperwork, and anyone can use it.

Attendees will get a 2-page reference card (“green card”), which lists all RISC-V extensions, to contrast this minimal ISA with the 3,600-page x86 manual and the 5,400-page ARMv8 manual.

We conclude by recapping 10 RISC-V chips built using Agile methods in just 4 years. They used Chisel, a new hardware design language that reduces design effort by greatly increasing reuse.