
Smart Vision Chip Fabricated Using Three Dimensional Integration Technology

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Abstract

The smart vision chip has a large potential for application in general purpose high speed image processing systems. In order to fabricate smart vision chips including photo detector compactly, we have proposed the application of three dimensional LSI technology for smart vision chips. Three dimensional technology has great potential to realize new neuromorphic systems inspired by not only the biological function but also the biological structure. In this paper, we describe our three dimensional LSI technology for neuromorphic circuits and the design of smart vision chips.

1 Introduction

Recently, the demand for very fast image processing systems with real time operation capability has significantly increased. Conventional image processing systems based on the system level integration of a camera and a digital processor, do not have the potential for application in general purpose consumer electronic products. This is simply due to the cost, size and complexity of these systems. Therefore the smart vision chip will be an inevitable component of future intelligent systems. In smart vision chips, 2D images are simultaneously processed in parallel. Therefore very high speed image processing can be realized. Each pixel includes a photo-detector. In order to receive a light signal as much as possible, the photo-detector should occupy a large proportion of the pixel area. However the successive processing circuits must become larger in each pixel to realize high level image processing. It is very difficult to achieve smart vision chips by using conventional two dimensional (2D) LSI technology because such smart vision chips have low fill-factor and low resolution. This problem can be overcome if three dimensional (3D) integration technology can be employed for the smart vision

chip. In this paper, we propose a smart vision chip fabricated by three dimensional integration technology. We also discuss the key technologies for realizing three dimensional integration and preliminary test results of three dimensional image sensor chips.

2 Three Dimensional Integrated Vision Chips

Figure 1 shows the cross-sectional structure of the three dimensional integrated vision chip. Several circuit layers with different functions are stacked into one chip in 3D LSI. For example, the first layer consists of a photo detector array acting like photo receptive cells in the retina, the second layer is horizontal / bipolar cell circuits, the third layer is ganglion cell circuits and so on. Each circuit layer is stacked and electrically connected vertically using buried interconnections and micro bumps. By using three dimensional integration technology, a photo detector can be formed with a high fill-factor and high resolution, because several successive processing circuits with large areas are formed on the lower layers underneath the photo detector layer. Every photo detector is directly connected with successive processing circuits (*ie.* horizontal and bipolar cell circuits) in parallel via the vertical interconnections. The signals in every pixel are simultaneously transferred in the vertical direction and processed in parallel in each layer. Therefore high performance real time vision chips can be realized. We considered the 3D LSI suitable for realizing neuromorphic LSI, because the three dimensional structure is quite similar to the structure of the retina or cortex. Three dimensional technology will realize new neuromorphic systems inspired by not only the biological function but also the biological structure.

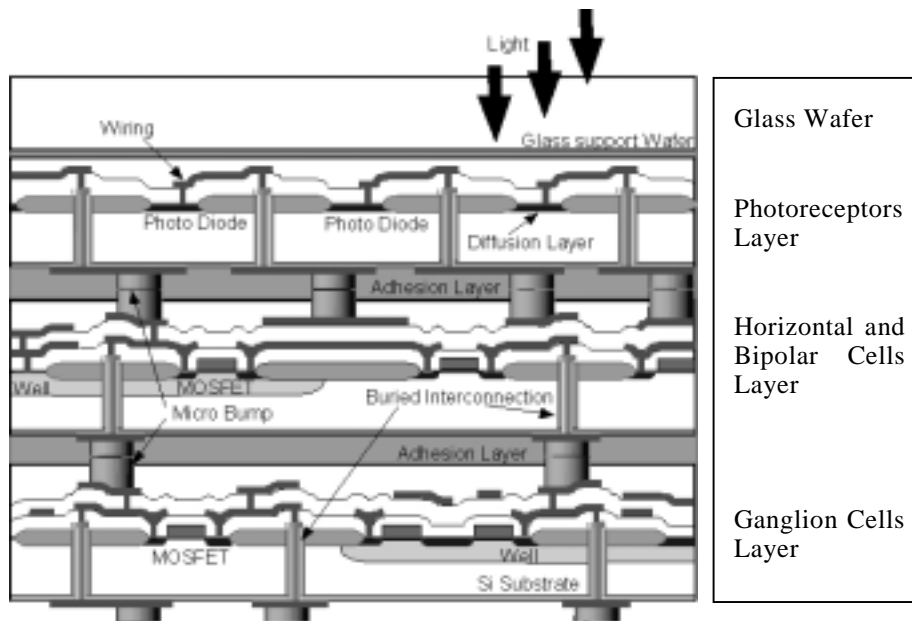


Fig.1 Cross-sectional structure of three dimensional vision chip.

Figure 2 shows the neuromorphic analog circuits implemented into 3D LSI. The circuits are divided into three circuit layers. Photodiodes and photocircuits are designed on the first layer. Horizontal / bipolar cell circuits and ganglion cells are on the 2nd and 3rd layer, respectively. Each circuit layer is fabricated

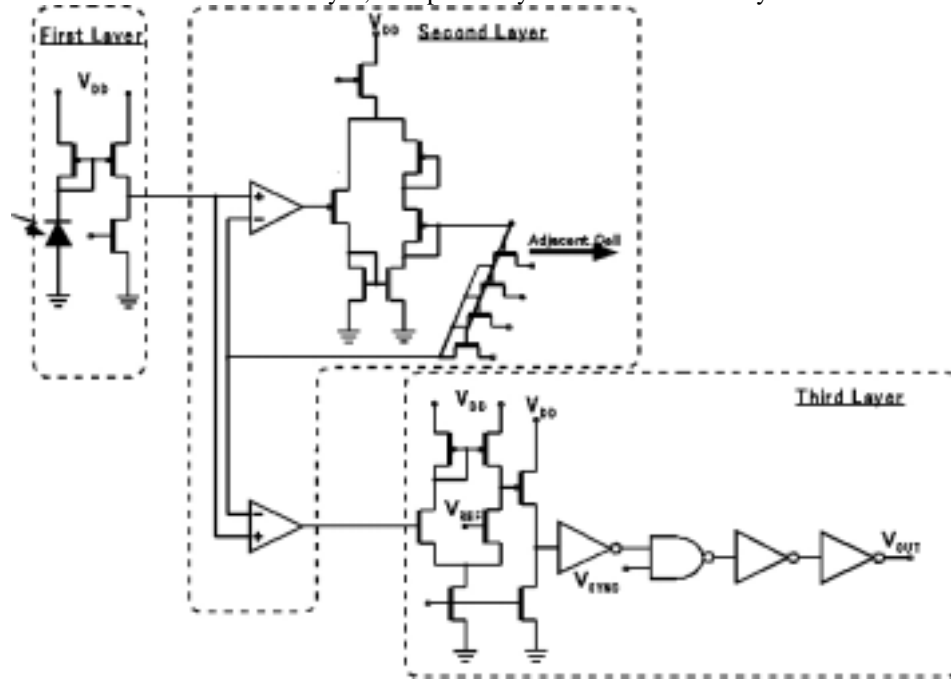


Fig.2 Circuit diagram of three dimensional vision chip.

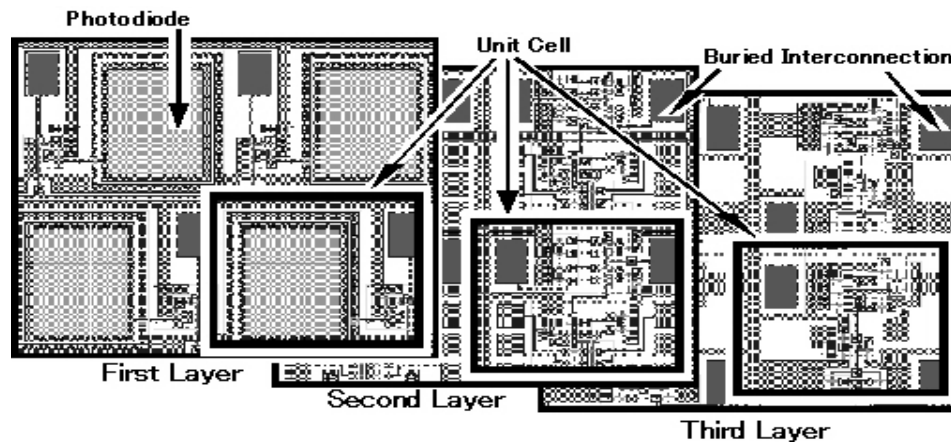


Fig.3 Layout of the three dimensional vision chip.

on different Si wafers and stacked into a 3D LSI. Light signals are converted into electrical analog signals by photodiodes and photocircuits on the first layer. The electric signals are transferred from the first layer to the second layer through the vertical interconnections. The operational amplifiers and resistor network on the

second layer act as horizontal and bipolar cells as proposed by C.Mead[2]. Then electric signals are further transferred through the vertical interconnection from the second layer to the third layer. The analog electric signals coming from the second layer are digitized by comparing with the reference voltage, V_{REF} . The output is driven by the buffers synchronized with V_{SYNC} . Finally, the output digital signals will be transferred to a V1 chip and so on. This 3D vision chip is designed with $1.5 \mu\text{m}$ CMOS technology. The fill-factor becomes 2.6 times larger than in 2D LSI. The large fill-factor can be easily achieved as shown in Fig.3.

3 Fabrication sequence and key technology for three dimensional integration

The fabrication sequence of the 3D chip is illustrated in Fig.4. The device wafer with the buried interconnections is glued to a quartz glass and then thinned from the backside using mechanical grinding and CMP (Chemical Mechanical Polishing). The micro bumps are formed on the bottom of the buried interconnections on the backside. This thinned device wafer is glued to another device wafer after a careful wafer alignment. By repeating this sequence, the 3D stacked wafer can be obtained. To achieve such a 3D chip, several key technologies such as formation of buried interconnection, micro-bumps, wafer thinning, wafer alignment and wafer bonding have been developed.

Deep Si trenches are required to form buried interconnections, which act as the vertical interconnections. The $2.5 \mu\text{m}$ Si trench with a depth of around $60 \mu\text{m}$ was formed using Inductively Coupled Plasma (ICP) etching. Then, the Si trench was oxidized and filled with n^+ poly-Si ($0.4\text{m}^{-1}\text{cm}$) by Low Pressure Chemical Vapor Deposition (LPCVD). The wafer must be thinned to around $30 \mu\text{m}$ from the backside surface using grinding and CMP techniques

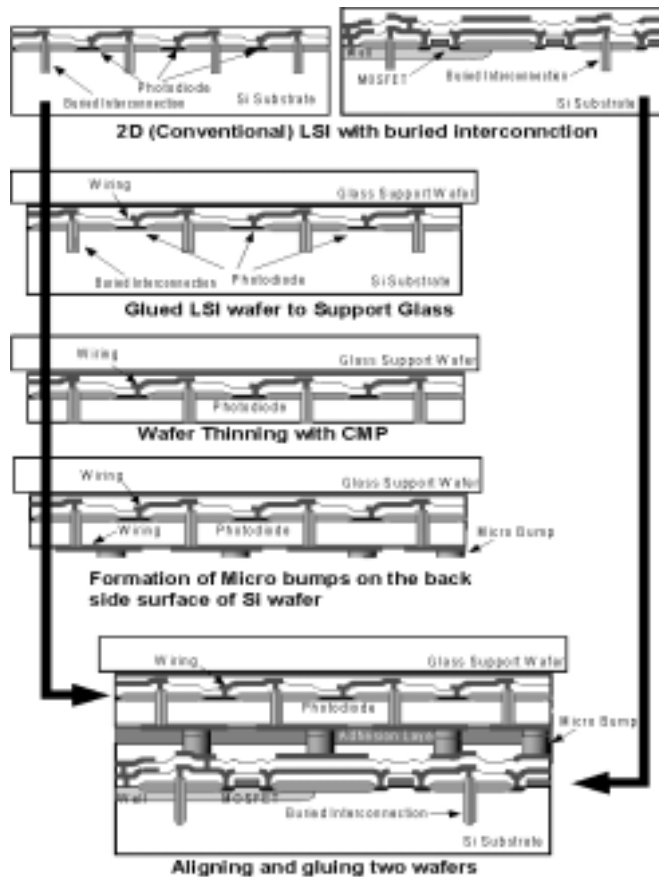


Fig.4 Fabrication sequence of 3D vision chip.

after it is bonded to the quartz glass which acts as a mechanical supporting material. Next, In-Au micro bumps are formed on the back surface using the lift-off technique after the deposition of insulation film. Then the thinned wafer is aligned to the bottom wafer with the alignment tolerance of $\pm 1 \mu\text{m}$ using a 3D wafer aligner. The 3D wafer aligner allows us to uniformly contact two wafers. In-Au micro-bumps are used to bond the two wafers. In order to enhance the bondability between them, we have developed an adhesive injection method. The liquid epoxy adhesive is injected into the gap between two wafers in a vacuum chamber after the temporary bonding using the micro bumps. The electrical connection between two wafers is achieved through the buried interconnections and micro-bumps. We investigated their electrical characteristics using several test patterns. The contact resistance of a bump with a size of $10 \mu\text{m}^2$ was very small and less than 0.1Ω . The resistance of the buried interconnection with the size of $2 \mu\text{m} \times 14 \mu\text{m}$ was less than 9Ω . A vertical interconnection chain consisting of 144 micro bumps and 144 buried interconnections could also be yielded. Figure 5 shows the current-voltage characteristics and the resistance of the vertical interconnection chain. The linear I-V curve was obtained.

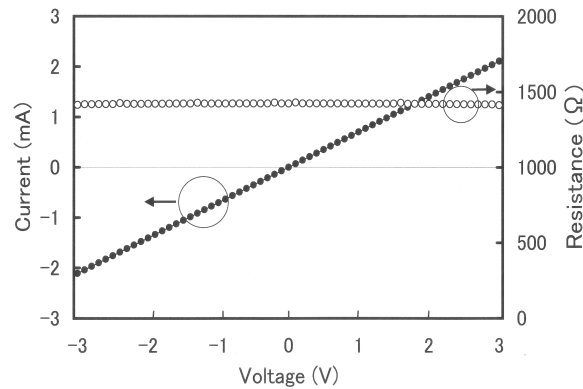


Fig.5 Electrical characteristics of buried interconnecton and micro bump chain.

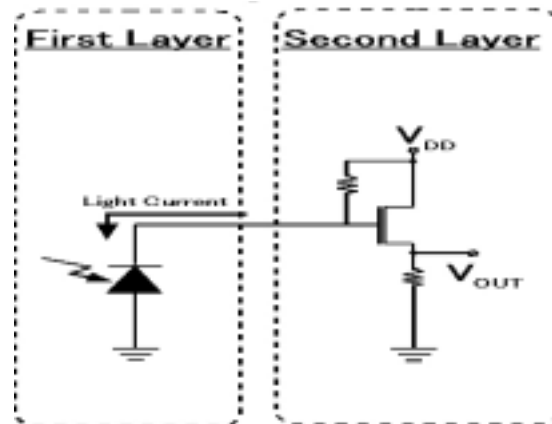


Fig.6 Configuration of 3D image sensor chip.

4 Three dimensional image sensor chips

We fabricated a 3D stacked image sensor chip with a simplified photocircuit and evaluated its electrical characteristics. Figure 6 shows the configuration of the image sensor chip. The photodiode image sensors and buried interconnections are formed on the first layer. MOSFETs are fabricated on the second layer. The photodiode on the first layer is electrically connected to the photocircuit on the second layer through the buried interconnections and micro-bumps. Figure 7 shows

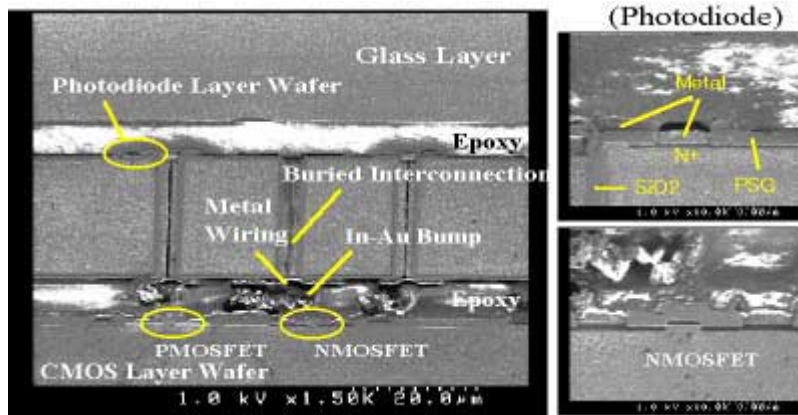


Fig.7 SEM cross section of 3D image sensor chip.

the SEM cross section of the 3D image sensor chip consisting of the two layers: image sensor layer and CMOS circuit layer. The first layer with the photodiode and buried interconnections and the second layer with the CMOS circuits are stacked on the glass layer which acts as a handling wafer during fabrication. It is clearly observed in this figure that the upper thinned silicon layer with the photodiode array is uniformly bonded to the lower CMOS circuit layer and these layers are connected through the buried interconnections and micro-bumps in a vertical direction. The electrical characteristics of this stacked 3D image sensor chip were evaluated. Figure 8 shows the evaluation result of the simplified image sensor circuit. The signal light was illuminated through the top quartz glass. As is obvious in this figure,

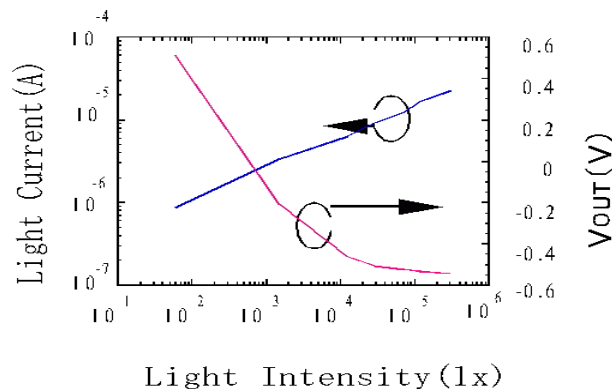


Fig.8 Output signal of 3D image sensor chip.

the reverse current of the photodiode is considerably increased by being irradiated with the signal light and hence the photodiode formed on the 3D image sensor chip is well operated. It is also demonstrated that a considerably large change in the output signal voltage of the photocircuit is obtained as the signal light is increased. From these results, we could confirm the operation of the 3D image sensor chip which was fabricated using our 3D integration technology.

5 Conclusions

We proposed the application of three dimensional integration technology for neuromorphic LSI. The three dimensional structure is quite similar to the retinal or cortex structure and a high fill-factor and highly parallel operation can be easily realized using 3D technology. Three dimensional technology will realize new neuromorphic systems inspired by not only the biological function but also the biological structure. A new 3D vision chip consisting of three layers was also proposed. A 3D image sensor chip was fabricated using this 3D integration technology and its basic electrical characteristics were evaluated. The electrical characteristics of 3D integrated LSI with the buried interconnections and micro-bumps could be confirmed as well.

Acknowledgments

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